THERMAL MANAGEMENT AND ELECTROMECHANICAL NOISE SUPPRESSION IN A PORTABLE JOSEPHSON JUNCTION VOLTAGE STANDARD

by

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ABSTRACT

NAMIT SINGH. Thermal management and electromechanical noise suppression in a portable Josephson junction voltage standard. (Under the direction of DR. JAMES F. CUTTINO)

A self-contained, fully portable, Josephson junction voltage reference standard system has been designed, developed and tested. The system relies on an active, closed-cycle refrigerator (CCR) cryocooler system and completely eliminates the reliance on liquid helium for cooling the Josephson Junction Array (JJA) chip to the required superconducting temperature of approximately to 4.2 K. The CCR based system has performance capabilities comparable to the liquid helium Dewar-based system and is packaged to operate as a portable system in environments like the US Army's calibration vans or calibration labs that do not have access to liquid helium.

The use of a CCR based cryocooling system brings forth many challenges not found in the classic Dewar-based system. This work identifies the principal challenges for achieving an operating system, and provides unique solutions to overcoming two areas of significant concern, thermal management and electromagnetic noise.

Dewar based systems provide three-dimensional convective cooling. While very effective in cooling, they are inappropriate for portable labs and are subject to evaporation. The challenge for an active system is in providing adequate thermal management to ensure sufficient cooling despite having only one-dimensional conductive cooling. An extensive study was conducted into various methodologies for mounting the chip in the new system and ensuring that superconducting temperatures were obtained. The surface roughness of a conventional machined surface is in the range of several

micrometers. The random peaks and valleys of the surface offer insufficient contact area between the cryocooler cold-head and the Josephson junction array chip, resulting in higher than superconducting temperatures at the JJA chip surface. Several approaches researched to increase the thermal contact conductance included thermal grease, adhesives and other high conductivity interstitial materials. The solution provided in this research is an elegantly simple technique, which eliminated the introduction of viscous materials or adhesives, thereby improving the maintainability of the chip. An innovative chip-mount was designed and machined using a state-of-the-art diamond turning technique to achieve a surface roughness of lower than 5 nm and completely eliminate the use of any foreign material. The diamond turned surface attained an operational temperature of 4.2 ± 0.2 K indicating a 30% improvement in the ability to cool the JJA chip.

The second area of interest is understanding the presence of magnetic fields and electromagnetic noise in the vicinity of the JJA chip and eliminating or greatly reducing them. High permeability MuMetal® magnetic shields were designed and installed to reduce the presence of magnetic field by up to 90%, and the nature of magnetic field noises were experimentally quantified. Performance deterioration due to the presence of electromagnetic noise induced by the cryocooler, motor and pump was expected, but for the first time detailed experiments were conducted to measure the magnetic fields in the system, understand their effects, and systematically eliminate or reduce them.

The final system was assembled and the performance was verified using standard Josephson voltage standard (JVS) system practices. A comparison of different operational parameters for the CCR based system was done with the laboratory based

liquid helium cooling system, and the results were found to be comparable. The values for critical current and the step amplitude for the JJA chip (# 2629B11) were reported by the chip manufacturer to be 110 μA and 29 μA, respectively, tested with a liquid helium system; the same values were measured to be 112 μA and 27 μA, respectively, while operating in the UNC-Charlotte JVS system. The measured values were within the experimental repeatability of 5% and the nature of characteristic I-V curves and voltage steps were similar to the measurements made in the liquid helium system. These comparisons demonstrated the operational capabilities of the UNC-Charlotte CCR based Josephson voltage standard system.

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LIST OF ABBREVIATIONS

APSL	Army primary standards laboratory
BCS	Bardeen-Cooper-Schrieffer
CCR	Closed-cycle refrigeration
DVM	Digital voltmeter
EMI	Electromagnetic interference
G-M	Gifford McMahon
GPS	Global positioning system
I-V	Current-Voltage
JJ	Josephson junction
JJA	Josephson junction array
JVS	Josephson voltage standard
NMI	National Measurement Institutes
OFHC	Oxygen free high conductivity
RF	Radio frequency
RFI	Radio frequency interference
SQUIDS	Superconducting quantum interference devices
TMDE	Test, measurement and diagnostic equipment

CHAPTER 1: INTRODUCTION

Today's US Army relies on increasingly sophisticated equipment and weaponry systems to provide the most accurate and efficient fighting force in the world. Unlike most of the weapons of the 20th Century, in today's world, most of the technologically advanced equipment and devices are electronically operated and controlled. The operational efficiency of these systems is directly dependent on the ability to accurately measure voltage for the purpose of calibrating the systems. This dissertation presents the work done in developing a portable voltage standard for use by the US Army Primary Standards Laboratory (APSL) to provide a field-ready standard for voltage against which in-service equipment could be calibrated. The voltage standard system presented here operates on the principle of the Josephson effect [1-4]. An integrated circuit chip consisting of an array of superconducting Josephson junctions produces a known constant voltage (10 volts or 1 volt, based on the chip), which is used as an intrinsic standard for voltage calibration. The focus of this work was to develop a fully operational prototype of the portable Josephson Voltage Standard (JVS) system and conduct a detailed investigation into determining and controlling all the factors affecting the stability of the system.

The portable JVS system relies on a Closed-Cycle refrigeration (CCR) system for cooling of the superconducting Josephson Junction Array (JJA) chip to the operating cryogenic temperature of 4.2 Kelvin. The stable operation of the JJA chip is highly dependent on the successful cooling of the chip and is very sensitive towards the presence

of any magnetic field or any electromagnetic noise in the measurement instrumentation. Design of the system presented here focuses on addressing these issues and successfully implements methods of eliminating or reducing these effects.

1.1 Research Motivation

The International System of Units, SI units, was established to meet the need for a worldwide set of units that is uniform and coherent. The SI units are categorized into seven base units such as length, mass, time, electric current, temperature, amount of substance and luminous intensity. Out of the seven base units, ampere (electric current) is the only unit that is related to electrical measurements. The unit of 'Volt' is defined in terms of current, length, mass and time as "that electromotive force between two points on a conductor carrying a constant current of 1 ampere when the power dissipated between the two points is 1 watt."[5]

Prior to 1972, a Weston cell [6] formed the primary voltage standard and measurements were made using techniques which drew negligible current from the standard. A standard Weston cell delivers a constant electro-motive force of 1.019 volts at 20° C and is usually kept immersed in a temperature controlled oil bath protected from vibrations. Figure 1.1 shows the diagrammatic representation of the Weston voltaic cell from the patent issued to Edward Weston [6] in April 1893, where he mentions, "I have discovered a voltaic cell, the temperature coefficient of which is practically invariable; in other words, a cell which is free from temperature error, or in which the electromotive force does not depend upon the temperature of the cell. While a cell of this character may be applied to various uses, it will find its practical employment and be of the highest utility as a standard of measurement of electromotive force. There is, at the present time,

no absolute standard of the unit of electromotive force, (the volt) but there is a variety of cells termed 'standards' with which comparisons are made." He discovered that the electromotive force of all cadmium salts is practically independent of temperature change. As seen in Figure 1, the cell contains an amalgam of cadmium and mercury as the anode and a mixture of pure mercury and proto sulphate of mercury as the cathode; both the cells are then filled with a saturated solution of cadmium sulphate. Obviously, the operation of the Weston cell is highly dependent on the involvement of chemicals. If no appreciable current is drawn from the Weston cell, it will retain its voltage for years, but drift and transportability limit the uniformity of the voltage standard to about 1 ppm [7]. The uncertainty of measurements associated with the Weston cell directly translates to the uncertainty and the instability of the SI volt.

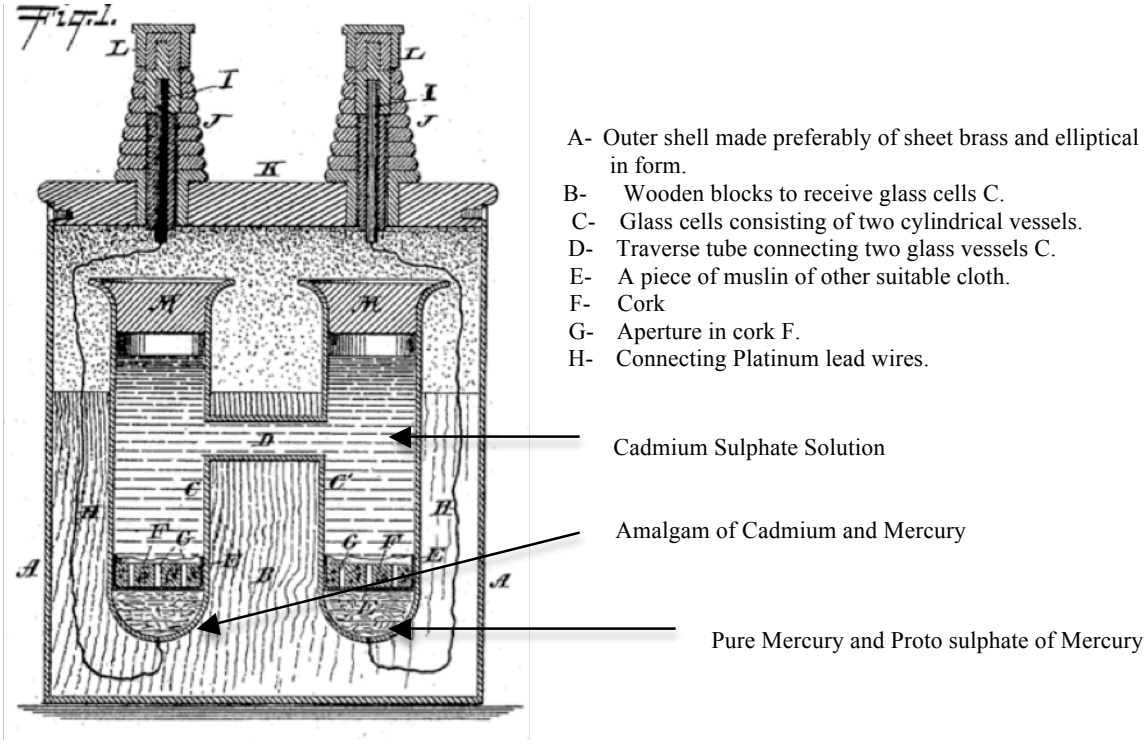


Figure 1.1: Diagrammatic representation of a Weston cell [6].

In order to achieve the SI volt, experiments were carried out that were difficult to conduct and produced results with unacceptable levels of uncertainty and non-repeatability [8-10]. By the 1970's, many national laboratories started using the Josephson effect as the practical standard of voltage [11, 12] and currently most of the national labs around the world maintain their own JVS systems [13-17]. The stability of a Josephson volt depends solely on the stability of the frequency of an oscillating current across the Josephson junction. Today, metrologists have developed artifacts and experiments representing the SI volt that are stable and reproducible to a level approaching 0.001 parts in 10^6 (ppm) [7]. Details about the operational physics of the Josephson junction and the discussion on Josephson effect are covered in Chapter 2; only the developmental milestones of voltage standards are discussed in this introduction. The development and acceptance of voltage standards over the years have been at different levels in different parts of the world. National labs and measurement institutes around the world were using and relying on different measurement standards for voltage [8-11, 18-19]. Figure 2 is a semilog plot giving an overview of how the differences in dc voltage measurement among National Measurements Institutes (NMI's) have decreased [7].

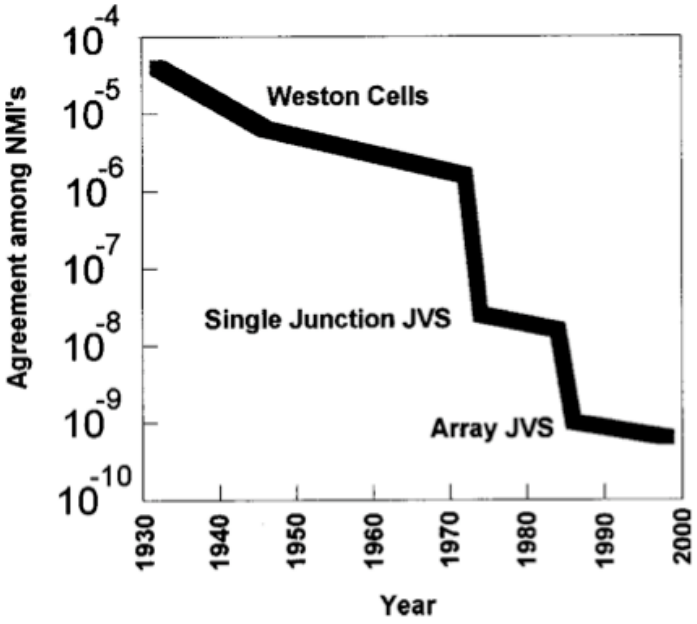


Figure 1.2: Approximate level of agreement in dc voltage measurements among National Measurement Institutes (NMI's) from 1930-2000 [7]

The single junction Josephson voltage standard provided a much more stable voltage reference compared to the Weston cell but were very difficult to operate as they generated a very small voltage, on the order of 1 to 10 mV [7, 11-12]. Attempting to raise the output voltage by connecting two or more junctions in series aided in developing a series-array Josephson junction. The first practical 1 V Josephson standard was produced in 1985 [7]. Further advances in the superconductive integrated-circuit technology resulted in the production of 10V Josephson junction array chips. Standards such as the Josephson volt that depend on fundamental constants rather than physical artifacts are known as intrinsic standards. Although the Josephson voltage standard (JVS) does not realize the SI definition of the volt, it provides a very stable reference voltage that can be reproduced anywhere [7].

The high accuracy metrology instrumentation involved with the voltage standard had been previously constrained to the laboratory environment because of various factors. The superconducting state of the Josephson array chip has historically been achieved by immersing the chip in liquid helium. Large volumes of liquid helium are stored in Dewars that are not suitable for mobile transfer. The low boiling point of helium (4.2 K) requires it to be stored under closed physical conditions. In order to maintain a constant level of helium in the Dewar, regular refilling is required. The constant replenishing of helium is a very expensive process and constrains the system to the locations that have abundant supply of liquid helium.

The United States Army Primary Standards Laboratory (APSL) recognizes the need for development of a transfer level calibration technology. The test, measurement and diagnostic equipment (TMDE) used by the US Army provides both fixed calibration operations situated on major Army posts and mobile calibration equipment used in the field on tactical calibration vehicles. The laboratory voltage standard incurs a lot of operational expenses because of the use of liquid helium, and in turn constrains the system to the non-transportable laboratory environment.

The United States Army TMDE and The University of North Carolina at Charlotte initiated a collaborative effort to develop a portable Josephson junction intrinsic voltage standard [20]. The goal of the project was to develop a prototype portable voltage reference standard system for installation in the Army's calibration van. The objective was to design a system that would operate independently of liquid helium and could be constructed by assembling off-the-shelf components, hence, simplifying component replacement.

1.2 Structure of Dissertation

The goal of this dissertation is to describe the development of the portable Josephson junction voltage standard system. The development of the operational prototype had many challenges associated with it. This dissertation is structured in such a way that it provides sufficient background for the reader to understand concepts related to the Josephson system and further details the factors affecting the development of and the proper operation of the Josephson voltage standard system.

The work contained in this dissertation is arranged in the following order: Chapter 1 provides an introduction to the field of voltage standards and further discusses the need for developing a prototype of the portable Josephson voltage standard system. This section provides an overview of the structure of the dissertation and topics covered in different sections. Chapter 2 provides an introduction to the voltage standards, briefly surveys the basic knowledge of superconductivity and physics behind the Josephson junction phenomenology and the basic structure of a portable Josephson voltage standard (JVS) system. The two most significant challenges with the design of the system are identified, namely, thermal management and magnetic field management. Chapter 3 further discusses the thermal management of the system, presenting an in depth analysis of the conduction cooling of the JJA chip and design of the CCR system. A mathematical model of the thermal system is developed and presented. In Chapter 4, a detailed analysis of the thermal contact conductance problem is addressed. The dependence of heat flow across the interfacing surface of the JJA chip and the cryo-cooler cold head was studied, and new mounting techniques were developed and tested. The operation and performance of a superconducting chip is highly dependent on the presence of any magnetic field in

the vicinity, so Chapter 5 specifically addresses the challenges of magnetic shielding to reduce static magnetic fields and electromagnetic noise in the measurement system. After the complete assembly of the Josephson voltage system, the required tests were conducted to display the required operation of the system. The results for the various tests performed to prove the competency of the cryocooler based system are shared in Chapter 6 and are compared with the results obtained from other liquid helium based Josephson voltage standard systems operating in the laboratory environments. Chapter 7 presents the conclusions from the work.

CHAPTER 2: VOLTAGE STANDARD

The United States Army TMDE is responsible for calibration of the plethora of electronic equipment used by the Army. To assure the proper operation and accuracy of measurements, the equipment needs to be periodically tested and calibrated. The extensive use of these systems and equipments necessitates the calibration to be conducted outside the laboratory environment. A compact and transportable Josephson voltage standard needed to be developed for installation in the US Army calibration vans. At the heart of the Josephson Voltage Standard (JVS) system developed at UNC Charlotte is a Josephson junction array (JJA) chip that utilizes the superconducting characteristics of the material to generate a constant and stable voltage. This chapter provides some background for understanding operation of the system and discusses the design of the prototype JVS system.

2.1 Introduction

Superconductivity has been a subject of great interest for scientists, with numerous challenges in understanding the phenomenon and developing new applications. Even though the advances in the field of superconductivity have produced many applications utilizing superconducting magnets, magnetically levitated trains, superconducting quantum interference devices (SQUIDS), etc. the field still remains highly dependent on the technological advancements in the field of cryogenics. The low temperature superconductive devices operate at temperatures close to 4 Kelvin and these temperatures

are achieved with the help of cryogenic refrigeration systems. On another front, there have also been tremendous developments in the area of high-temperature superconductors with some materials with critical temperatures in the range of 130 K. The cooling of metals well below room temperature causes a significant reduction in the electrical resistance. Also, as the material approaches a temperature close to absolute zero, the energy of the material becomes very small and the flow of electrons in the conductor becomes negligible.

In 1911, Heike Kamerlingh Onnes [21] found out that steadily lowering the temperature of a mercury wire lowered the electrical resistance, and at 4.2 K, the resistance completely vanished. This characteristic state of no-resistance and pure conductivity achieved at a very low temperature was termed as the supraconductive state (now, commonly called superconductive state) and the materials displaying this extraordinary electrical property were called Supraconductors [21]. At extremely low temperatures, the overall energy of any material becomes very low; this change in the behavior causes the sudden drop in electrical resistance to diminishing values. At these temperatures the conduction of electricity in certain materials increase and hence the materials are known as superconductors. Onnes was awarded the Noble prize in physics in 1913 for his investigations on matter at low temperatures [22].

2.2 Principles of Superconductivity

After the discovery of superconductivity by Onnes in 1911, the behavior of superconductivity was observed in many metals but there was a lack of clear understanding of the phenomenon and a satisfactory explanation at the microscopic level was not provided until late 1950's. In order for scientists to explore the nature of

superconductors or develop applications based on the behavior, it was necessary to understand the phenomenon in detail. In 1937, Fritz London, recognized that supraconductors are macroscopic quantum systems and are a result of manifestation of quantum phenomena on the scale of large objects [23-25]. In 1957, a satisfactory explanation of the superconducting behavior was given at the microscopic level by John Bardeen, Leon Cooper and Robert Schrieffer [26-27]. They were awarded a Nobel Prize in physics in 1972 for their in-depth explanation of the phenomenon of superconductivity based on the quantum mechanical behavior of electrons and the theory was named as the BCS theory of superconductivity.

BCS Model of superconductivity:

The behavior of electrons is vastly different in a superconducting state as compared to normal conductors. In a conductor, the electrical resistance causes loss of energy in the form of heat. As the electrons pass through the conductor they collide with impurities and imperfections in the crystal lattice and loose energy in the form of heat. Cooper [28] realized that atomic lattice vibrations were directly responsible for unifying the entire current. They forced the electrons to pair up and could pass all of the obstacles that caused resistance in the conductor. These pairs of electrons are known as Cooper pairs. Cooper and his colleagues knew that electrons which normally repel one another must feel an overwhelming attraction in superconductors. The answer to this problem was found to be in phonons, packets of sound waves, present in the lattice as it vibrates [29, 30].

According to the BCS theory, [26, 27] as one negatively charged electron passes by positively charged ions in the lattice of superconductor, the lattice distorts. This in turn causes phonons to be emitted, which forms a trough of positive charges around the

electrons. Before the electron passes by and before the lattice springs back to its normal position, a second electron is drawn into the trough. It is through this process that two electrons, which should repel one another, link up as a pair. The forces exerted by the phonons overcome the electron's natural repulsion. The electron pairs are coherent with one another as they pass through the conductor in unison. The electrons are screened by the phonons and are separated by some distance.

When one of the electrons that make up a Cooper pair passes close to an ion in the crystal lattice, the attraction between the negative electron and the positive ion cause a vibration to pass from ion to ion until the other electron of the pair absorbs the vibration. The net effect is that the electron has emitted a phonon and the other electron has absorbed the phonon. It is this exchange that keeps the Cooper pairs together. It is important to understand, however, that the pairs are constantly breaking and reforming. Because electrons are indistinguishable particles, it is easier to think of them as permanently paired. Figure 2.1 illustrates a wave of lattice distortion due to attraction to a moving electron pair. The figure also illustrates how two electrons forming a called Cooper pair become locked together. By forming a pair of two the electrons pass through the superconductor more smoothly.

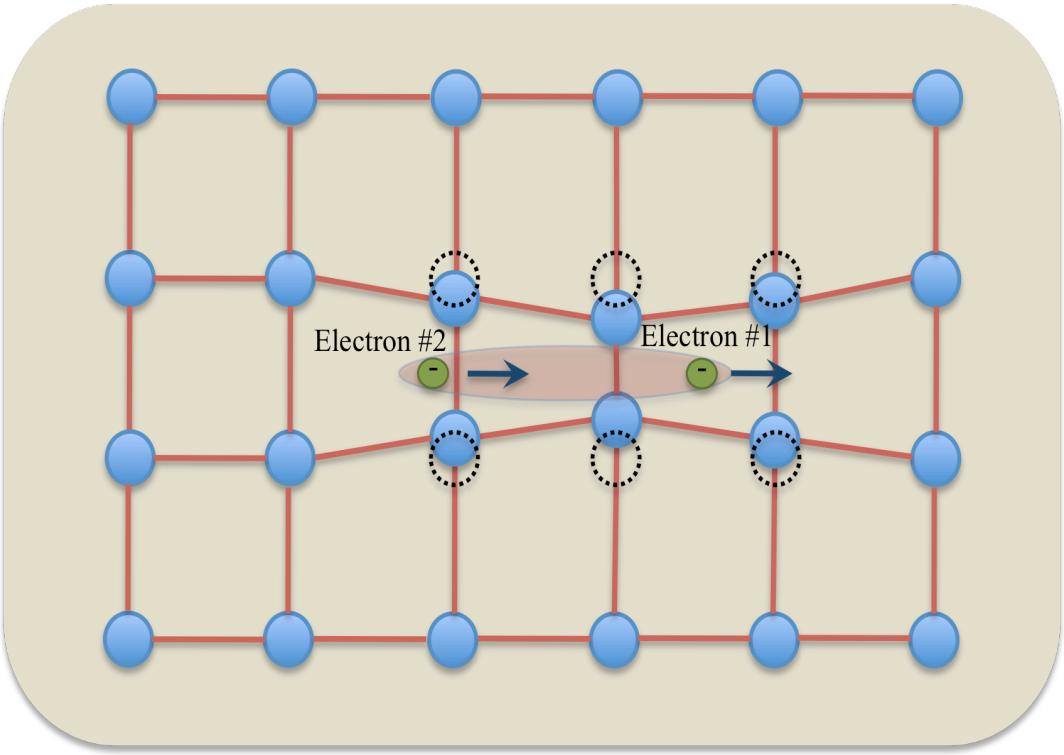


Figure 2.1: Lattice distortion and electron Cooper pairs in superconductors.

The BCS theory provided a much deeper understanding in the phenomenon of superconducting behavior and was widely accepted as a valid explanation. When the atoms of the lattice oscillate as positive and negative regions, the electron pair is alternatively pulled together and pushed apart without a collision. The electron pairing is favorable because it has the effect of putting the material into a lower energy state. When electrons are linked together in pairs, they move through the superconductor in an orderly fashion. The average distance between the paired electrons is called the coherence length, ξ. The temperature, current density and magnetic field are the most important parameters to be considered for a superconductor. The Cooper pair can be broken by increasing the energy of the pair by thermal (critical temperature), kinetic (critical current density) or magnetic (critical field) interactions. As long as the superconductor is cooled to very low temperatures, the Cooper pairs stay intact due to the reduced molecular motion. As the

superconductor gains heat energy the vibrations in the lattice become more violent and break the pairs and as they break, superconductivity diminishes. The temperature, current density and magnetic field forms a *phase space,* in which the particular material exhibits superconducting characteristics.

Meissner Effect:

In 1933, Walther Meissner and R. Ochsenfeld [31] discovered a very interesting property displayed by superconductors. According to their findings, when a material is in the superconducting state, it does not allow a magnetic field to penetrate the superconductor. The magnetic lines incident on the superconductor cause a generation of electric current on the surface, which in turn causes magnetic field generation inside the superconductor that balances the field. The Meissner effect is displayed only for small values of the magnetic fields; at higher values, the field penetrates into the material and causes the loss of superconductivity.

Brian Josephson:

In 1962, Brian Josephson, then a graduate student at the Royal Society Mond Laboratories, Cambridge, England, made an intriguing discovery in the field of superconductive tunneling [1]. After listening to a series of lectures from Professor Phil Anderson, a pioneer in the subject of tunneling supercurrents, Josephson was fascinated by the idea of "broken symmetry" in superconductors [2, 32, 33]. He then theoretically predicted and published his theory proposing an approach to the calculation of tunneling supercurrents between two metals when both metals are superconducting [1, 3, 4].

The subatomic elementary particles like electrons display the quantum mechanical properties of both wave and particle. According to the theories, the waves can penetrate a

thin barrier which, based on the classical particle theory, would not be possible for an electron. If a thin layer of insulator separates two metals, the insulator should act as a barrier for the moving charge carriers in the metals. But, Josephson observed that instead of blocking the flow of electrons, occasionally there is a certain fraction of electrons that would mischievously penetrate through the forbidden region. This tunneling of the electrons through the forbidden region arises from the wave nature of the electron and causes a flow of weak current known as the tunneling supercurrents [3, 4, 33]. Brian Josephson's discovery in the field of quantum interferometry theoretically explained the influence of applied electric and magnetic fields to influence and control the flow of tunneling supercurrents. Later, the theory proposed by Josephson was experimentally confirmed by different groups [2, 33]. This phenomenon of tunneling supercurrents through a junction of two superconductors separated by a thin insulating barrier is known as the Josephson effect. The discovery of Josephson effect revolutionized many aspects of electronics and Josephson was rewarded with the Nobel Prize in Physics in 1973 for his pioneering research discoveries of tunneling phenomenon in solids.

Physics of Josephson effect:

The electrons tunneling from one superconducting region to the other through an insulating barrier can penetrate the barrier without any voltage drop. This junction of weak electrical contact between two pieces of superconducting metal displaying the Josephson effect is commonly termed as a Josephson junction (JJ).

As materials are cooled down to a very low temperature, approaching absolute zero, some of them undergo a transition of material properties and start behaving as superconductors. If the material is cooled below its transition temperature, (T_c), the

electrical resistance of the material drops to a very low value. The density of current that flows through the junction is characteristic of the geometry and material of the junction[7].

When two superconductors are physically separated from each other, the electrons in each of them behave independently. The superconducting phase of the material is a position dependent parameter. Now, if the two superconductors are brought to within about 30 Å, single electron tunneling causes an exchange of quasiparticles [34]. Further, if the distance of separation is reduced to 10 Å, there is also a flow of Cooper pairs from one superconductor to the other causing the Josephson tunneling. In this situation the whole system of the two superconductors separated by the thin (~10 Å) dielectric barrier behaves to some extent as a single superconductor [26, 27, 34]. The electron pairs in the junction, tunnel through the barrier and cause a current flow. If the current flowing through the junction is lower than the critical current (I_c) there is no resistance against the flow and the voltage drop across the junction stays zero. If there is a magnetic field present in the region, it lowers the critical current of the Josephson junction. The lowering of the critical current doesn't affect the actual current flowing through the junction but the junction then develops a resistance to the flow because the actual current is now more that the critical current of the junction.

2.3 Josephson Junction Voltage Standard

Modern instrumentation requires very precise voltage measurements with high repeatability. Adopting the Josephson voltage standard (JVS) as the intrinsic standard for voltage fulfilled the need for such an accurate and stable measuring standard. The voltage standard currently adopted in the industry reproduces a unit volt by a quantum standard based on the Josephson effect [7-12]. Fundamentally, the Josephson effect is due to

tunneling of Cooper pairs formed by bound pairs of electrons occupying states with equal and opposite momentum and spin. The passing of a flux quanta through the Josephson junction of two weakly coupled superconductors produces a voltage across the junction. The flux quanta can be represented by

$$\phi = \frac{h}{2e} \tag{2.1}$$

where, *h* denotes Planck's constant and *e is* the elementary charge. Note that *2e* represents the charge of the electron pair. Among the many predictions that Josephson made associated with the tunneling of electrons, the most significant was the relation between the application of an oscillating current across the junction and the generation of a DC voltage. He stated that when a DC voltage, *V*, is applied across two superconductors separated by a thin insulating barrier, an oscillatory current, of frequency *f*, is generated across the junction, as shown in Equation 2.2 [3, 4].

$$f = \frac{V}{\phi} \tag{2.2}$$

Using state of the art time references, such as the cesium atomic clocks, the measurement of frequency can be precisely and accurately controlled. The Josephson effect thus reduces the production of voltages to the determination of a frequency. If the junction is operated at a non-zero voltage, *V*, it acts as an oscillator of a known frequency, thus a Josephson junction is an ideal voltage controlled oscillator. The voltage-to-frequency conversion constant, also known as the Josephson constant, K_J, has a value of [7]

$$K_J = 483{,}597.9\frac{GHz}{V} \tag{2.3}$$

The very high frequency and low voltage of this oscillation made it very difficult to

observe and measure. However, when an ac current at frequency *f* is applied to the junction, the junction oscillation tends to phase-lock to the applied frequency.

If during the phase-lock, the Josephson junction is irradiated with a microwave frequency *f,* the flow of flux quanta (known as the ac Josephson effect) produces constant voltage steps at a voltage V_n [7, 35].

$$V_n = n\frac{h}{2e}f \tag{2.4}$$

Usually the junction also phase-locks to the harmonics of *f*, resulting in a series of steps represented by *n* (*n* = 1, 2, 3, . . . denotes the integer step number representing the number of flux quanta which are transferred by each period of the microwave). These steps are a characteristic of the Josephson junction and can be seen on the Current-Voltage (I-V) curve. Figure 2.2 is the representation of the I-V characteristic of a typical Josephson junction with microwave power applied to it.

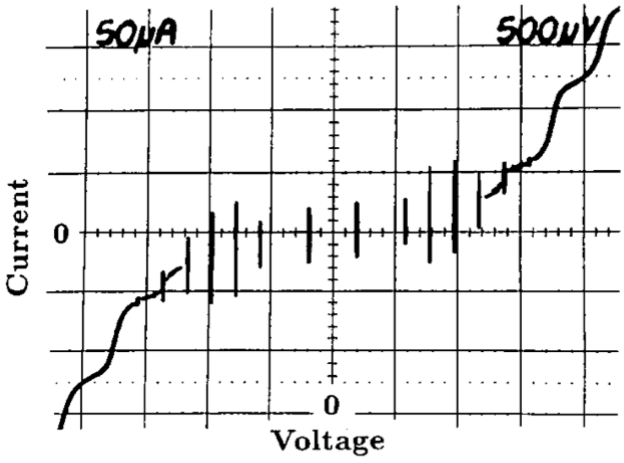


Figure 2.2: I-V Characteristic of a single Josephson Junction with 96 GHz microwave power applied [7].

The effects of microwave on the Josephson junction were experimented with by several groups and a detailed understanding was developed [36-39]. In adopting the ac Josephson effect as a practical standard of voltage, it was necessary to specify the exact value of the Josephson constant, $K_J = \frac{2e}{h}$, as that was the constant used in translating the value of frequency to voltage. Initially, many national laboratories used the ac Josephson effect to measure the more accurate value of 2e/h [11, 12, 18, 19]. By the early 1970's, most of the laboratories started using the ac Josephson effect as the practical standard of voltage [7]. Effective January 1, 1990, the new international definition of the practical unit of voltage was accepted and adopted by all standards laboratories and is given by [18]

$$V = \frac{nf}{K_{J-90}} \tag{2.5}$$

with, $K_{J\text{-}90} = 483\ 597.9\ \frac{GHz}{V}$. The uncertainty of $K_{J\text{-}90}$ is 0.4 ppm.

The discovery of a single Josephson junction and its capability to produce a highly stable voltage was a major breakthrough in the field of voltage standards. One of the biggest problems with the single junction voltage standard was that in the conventional operating mode the amplitude of the output voltage was in the order of millivolts. The thermal voltages induced by the temperature difference and other noise sources induced a major source of uncertainty in the measurement of standard cell voltages. The Josephson voltage standard was improved by connecting several junctions in series to produce larger quantized voltages. A single Josephson junction typically produces a quantized voltage from 1 mV up to 5 mV when driven with microwaves near 10 GHz [7]. Creating an array of Josephson junctions in series generated higher voltages, but these experiments had their own problems associated with stability, microwave distribution among junctions,

etc. A joint effort between the National Bureau of Standards (NBS) in the USA and the Physikalisch-Technische Bundes-Anstalt (PTBA) in Germany resolved these problems and created the first large Josephson junction array in 1984 [7].

To achieve measurable quantities of voltage using the Josephson junctions, highly integrated series arrays are used to achieve output voltages of 1 V or 10 V. These Josephson Junction Array (JJA) voltage standards can consist of up to about 20,000 Josephson junctions for a 10 V JJA chip. In order to obtain the largest voltage value from the smallest number of junctions, the junction array is designed in such a way that it delivers uniform microwave power to most of the junctions. Figure 2.3 is a diagrammatic representation of the JJ arrays fabricated on a silicon wafer using highly advanced micro-fabrication techniques. The series of superconducting junctions on the Josephson chip consists of microwave striplines that can propagate microwave power with relatively low loss.

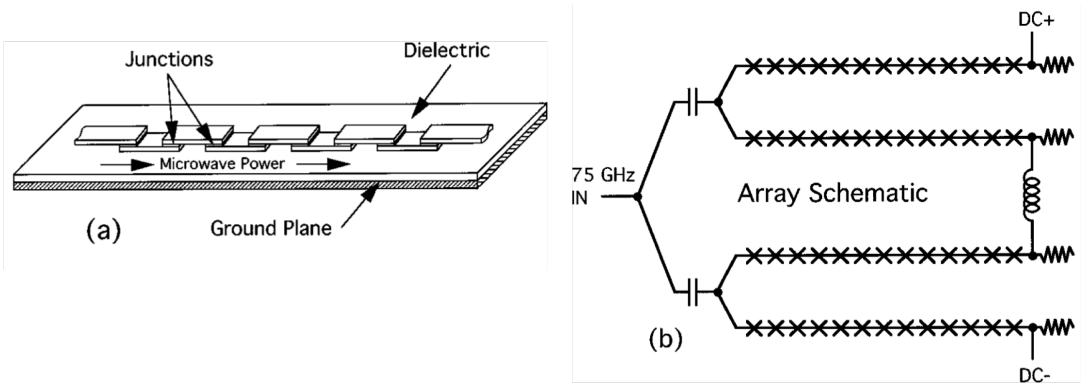


Figure 2.3: Diagrammatic representation of Josephson Junction Array and the circuit. [7]

Several national and military standard laboratories around the world are now using the Josephson junction array (JJA) voltage standard system because it provides very high accuracy and least uncertainty in calibration [13-17]. However, for the JJA chip to achieve the required operating temperature, majority of the laboratory designs incorporate large

volumes of liquid helium. Use of liquid helium Dewar to cool the JJA chip restrains the voltage standard system to the laboratory environment, typically requires significant manual interaction and increases the operating cost of the system. This research focuses on developing a portable Josephson voltage standard system that operates without the use of liquid helium to cool the chip, has the same or better operating accuracy as that of a laboratory installed liquid helium based system, provides a more consistent cool-down cycle to prevent trapping of magnetic flux, and offers the mobility that allows equipment to be transported to the field.

2.4 Dewar-based Voltage Standard system

A schematic of a typical liquid helium Dewar based Josephson voltage standard system is shown in Figure 2.4. As shown in the figure, the primary components are: Cryoprobe to hold the Josephson junction array (JJA) chip, JVS controller 1002, Phase Matrix 578 microwave counter for frequency phase locking, oscilloscope, computer and the scanner along with check standards and other device under test (DUT).

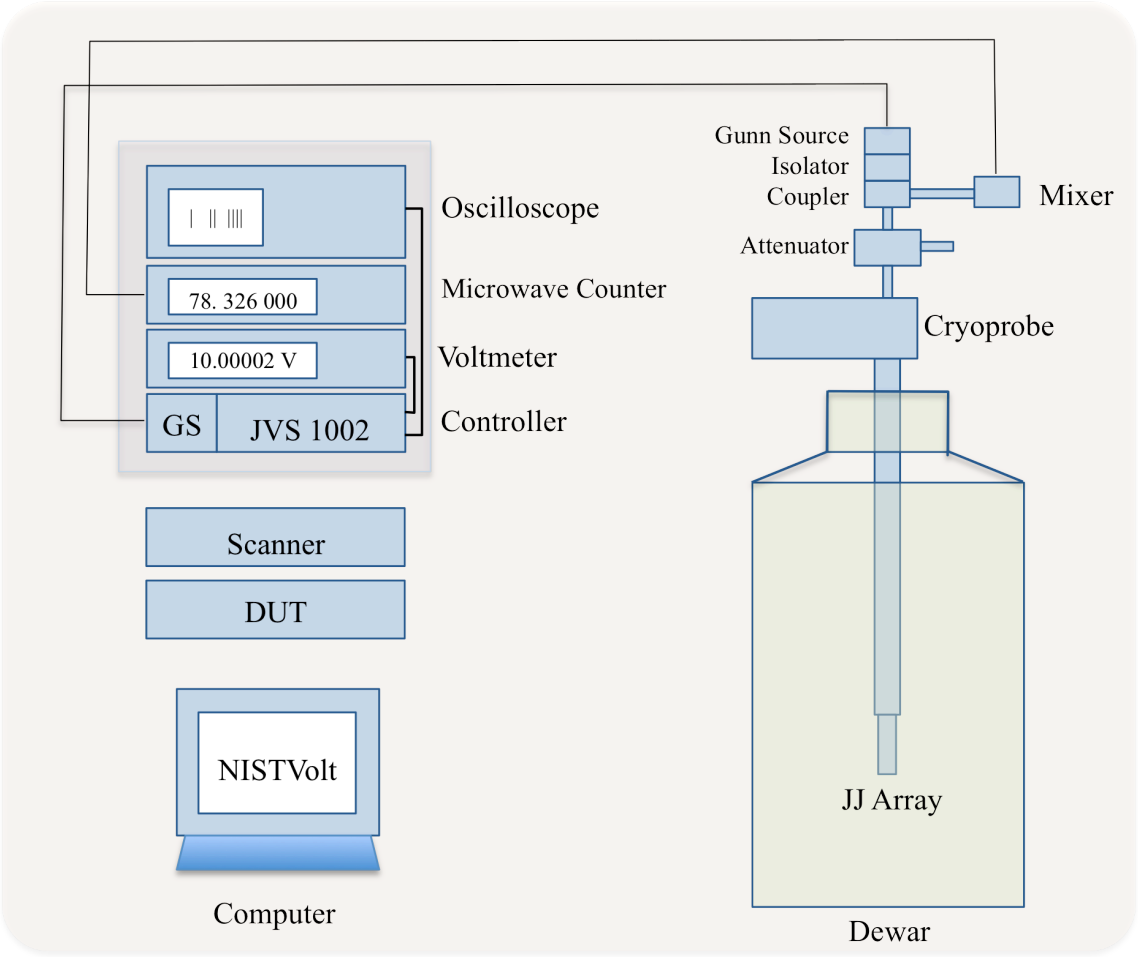


Figure 2.4: Liquid helium Dewar based Josephson voltage standard system.

From the operational point of view, the components can be categorized as a) the thermal system, b) magnetic shielding and electromagnetic noise suppression, c) microwave source, and d) measurement equipment. In designing an active system, the thermal system is of principal interest; however, significant modifications are also required for the shielding components since the cryocooler is an electromagnetic device and induces noise. These modifications are discussed in the following sections.

2.5 Design of a Portable System

Like the Dewar-based system, a cryocooler based portable JVS system consists of

most of the same components; however, significant development is required in the areas of thermal management and electromagnetic noise suppression. In the Dewar system, the chip is submerged in liquid helium, which provides three-dimensional cooling. Once the JJA chip is submerged in liquid helium it maintains a uniform temperature of 4.2 K, till there is sufficient liquid helium present in the Dewar. Once the level of liquid helium starts to drop, the superconducting junctions start to heat up and this can be seen in the operational performance of the JJA chip. In case of the CCR based JVS system, the JJA chip is mounted on a chip mount, which is attached to the second stage of the cryocooler, operating at 4.2 K. During regular operation of the cryocooler, the chip mount reaches a temperature of 4.2 K and the JJA chip is cooled by conductive heat transfer. The surroundings of a JJA chip are maintained under a state of vacuum, because of which there is no thermal convection. Under this situation, cooling of the JJA chip is through surface contact between the JJA chip and the chip mount. The thermal, magnetic, microwave and measurements systems are briefly discussed in this section, and at the end an overview of the complete assembled system is provided.

2.5.1 Thermal and Cryogenic System

The Josephson junctions are made of superconducting materials (niobium, in our case) that display their characteristic superconducting properties only when cooled below their critical temperature of 9.2 K. So, one of the most critical components while constructing a voltage standard system operating on the principle of Josephson effect is the cryogenic system. The cryogenic system is solely responsible for achieving the operating temperature of 4.2 K for the stable operation of the Josephson junction array (JJA) chip. At the heart of the cryogenic system is a closed circuit refrigeration unit

consisting of a Sumitomo cryocooler cold head (RDK-415D) [45, 46] and a Sumitomo compressor unit (CSA-71A) [47]. The cryocooler system cold head is a two-stage Gifford-McMahon (GM) cycle cryo-refrigerator. The function of the cold head is to produce continuous refrigeration at temperatures in the range of 25 K - 40 K at the first-stage cold station and in the range of 3.5 K – 4.2 K for the second stage cold station, based on the heat load of the system [45-47]. The cryocooler is enclosed in a cylindrical vacuum chamber constructed of aluminum. An Alcatel mechanical roughing vacuum pump is connected to the chamber with a capability of achieving a vacuum of $1x10^{-3}$ Torr. The JJA chip is secured on a precisely designed and machined Oxygen Free High Conductivity (OFHC) copper chip mount and the chip mount is mounted on the 4 K cold head of the cryocooler. The instrumentation of the system is connected to the JJA chip using a set of six wires (AWG-32). The six wires are soldered to a FR-4 fingerboard that establishes contact with the pads on the JJA chip and are used for biasing the chip and measuring the voltages. All the wires are thermally anchored at the 4 K stage and the 50 K stage to reduce thermal load. The detailed design of the chip mount and the JJA chip holder is discussed in Chapter 3. Inside the vacuum chamber a thermal radiation shield is used to eliminate the radiation heating of the JJA chip and other crucial components. The CCR system for cryocooling delivers the compressed helium gas to the cryocooler unit and achieves the temperature essentially same as that of a liquid helium based system, without the involvement of handling liquid helium. An in-depth discussion is provided on the complete assembly and design of the cryocooling system in Chapter 3.

2.5.2 Magnetic Shielding

The operational performance of a Josephson junction is dependent upon the presence of any external magnetic fields. The presence of magnetic fields higher than a critical value for the particular superconducting material prevents the material from achieving the superconducting state. As the temperature of the Josephson junction is lowered below the critical temperature, any magnetic field present in the vicinity of the junction can cause magnetic 'flux trapping'. As the junction transitions into the superconducting state, due to the Meissner effect, eddy current loops start forming within the junctions and can cause trapping of magnetic flux. Any magnetic field greater than the critical field of the superconductor prevents the circuit from entering the state of superconductivity.

The best way to avoid magnetic flux trapping is to create a magnetically shielded region around the JJA chip and to cool the chip at a slow and constant rate. The voltage step transitions are very sensitive to any induced noise; hence, all the wires go through an RF-filter box and all the other electronic components are grounded. The complete details about the design of magnetic shields and RF filters along with the results for the performance are presented in detail in Chapter 5.

2.5.3 Microwave Source

The characteristic equation for a Josephson junction, $f = 2eV/h$, represents the frequency at which the current oscillates when a dc voltage, V, is applied across the junction. The oscillating current in the junction has a very high frequency and low magnitude. Because of the nature of this current, it is very difficult to measure it directly, hence, an ac voltage of a known frequency f is applied to the junction and the oscillation phase-locks to the applied frequency and provides a very stable reference voltage.

The microwave energy required to operate the Josephson junction chip is generated by a Gunn diode oscillator operating in the range of 77 GHz $\pm$ 2 GHz. Since, the performance of a Josephson voltage standard is dependent on the stability of the frequency source, a very low-noise and stable operation of the millimeter-wave source is necessary. The system is designed to phase lock the millimeter-wave Gunn diode oscillator synchronized to an external reference source operating at 10 MHz. An EIP Model 578B Source Locking Microwave Frequency Counter [48] is used to perform the frequency measurement as well as phase lock the external signal source. The EIP-578B has the capability of either using an external frequency source or the internal time base crystal oscillator can be selected to maintain a long-term accuracy and stability. The external reference source used for the system is a Datum Inc. manufactured ExacTime ET 6000-75 GPS Time Code and Frequency Generator [49]. The ET-6000 contains a voltage controlled Crystal oscillator; the Global Positioning System (GPS) Timing Unit includes the GPS Main module, an antenna and a coaxial cable for interconnections. The GPS Timing Unit determines time and frequency by measuring the time of arrival of the precise timing mark and monitoring time and frequency data from the Navstar satellite constellation [49]. The GPS Unit provides a corrected 1 pps output signal and a 10 MHz Sine wave [49]. The 10 MHz signal output from the GPS unit is provided to the EIP-578B locking counter as the external reference by connecting a coaxial cable from the back of the GPS unit (connector J6) to the back of the EIP (connector J5, 10 MHz Timebase-Ext).

The external frequency reference is utilized to obtain an accurate and stable output from the Gunn diode oscillator. The Gunn assembly consists of the Gunn diode, an isolator, a coupler, a mixer and an attenuator. Figure 2.5 shows a picture of the Gunn

assembly. The Gunn diode is connected to the Gunn Oscillator Power Supply (GS1002)[50] by a coaxial cable and controls the output frequency of the Gunn diode by adjusting the supplied voltage from the GS1002. The isolator attached right next to the Gunn diode prevents any feedback to the Gunn diode. The coupler and the mixer are an essential part of the lock-in subsystem; the output from the mixer is fed to a frequency counter (EIP 578B), which determines the frequency of the signal, and the difference in frequency is used to send a signal to the Gunn Oscillator Power Supply (GS1002) controller that adjusts the bias voltage sent to the Gunn diode to vary its output frequency. This iterative process compares the frequencies between the reference and the local oscillator to stabilize the local oscillator to the reference. An attenuator adjusts the power output of the system and the output from this system is delivered to the JJA chip through an assembly of waveguides.

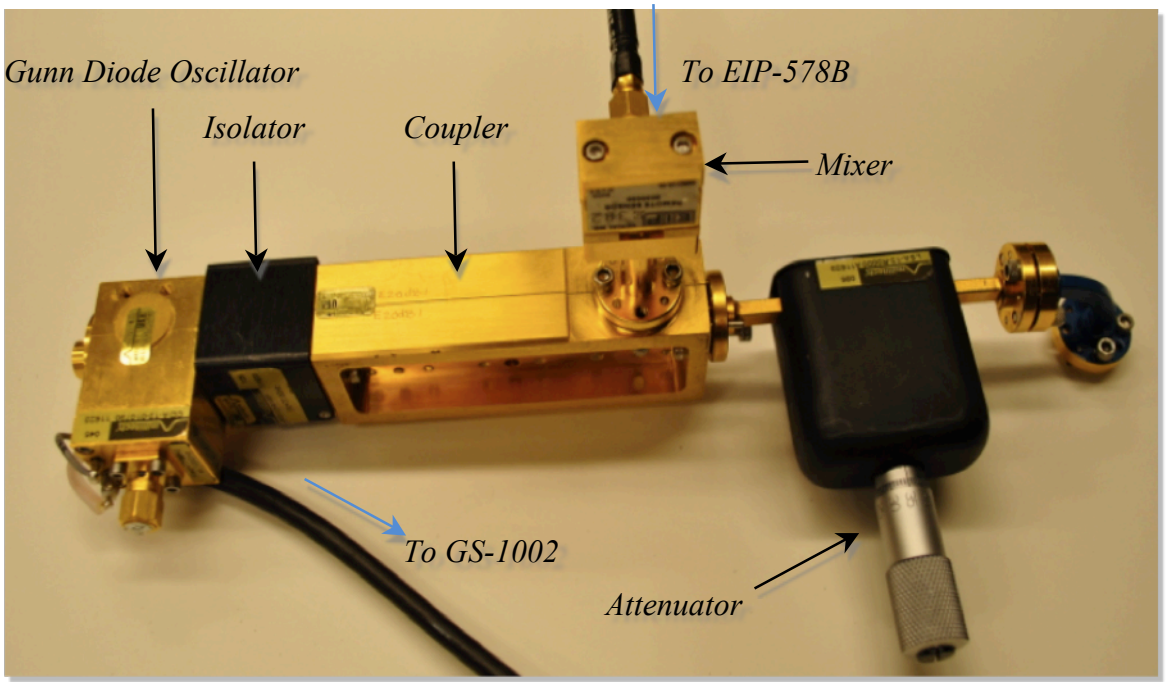


Figure 2.5: Gunn Diode assembly

2.5.4 Layout of the Portable System

In the previous section, different subsystems of the Josephson Voltage Standard system were introduced and briefly discussed. This section presents an overview of the complete design layout of the portable JVS system. Figure 2.6 gives a diagrammatic representation of the complete assembly along with the connection and wiring diagrams. All the components of the system are housed in a standard rack of approximate dimensions 56 cm x 82 cm x 195 cm. The bottom half of the rack contains the refrigeration unit for the cryocooling system including the compressor, radiator and cooling fan along with other electronic components for the operation of the cryocooler. The top half contains the vacuum chamber that encloses the two stages of cryocooler (cold end) and the assembly holding the Josephson Junction Array (JJA) chip. The pump for circulating compressed helium through the cryocooler is attached at the top end of the vacuum chamber and is connected to the compressor unit with flex-line for transporting helium. The cryocooler pump circulates the compressed helium gas through the cryocooler tubes to cool the cold head and the JJA chip. The chamber is connected to the vacuum pump that creates a vacuum of close to 1 mTorr during the operation of the system.

All the instrumentation components of the system are stacked in the top portion of the rack with their front panel completely accessible to the operator. The connection of these components can be seen in Figure 2.6. A GPS antenna installed at the roof of the building acquires accurate data of time and frequency and transmits it to the GPS receiver (ET-6000-75). Using the external reference obtained from the GPS system, the millimeter wave subsystem (consisting of EIP 578B, the Gunn diode assembly and the GS 1002)

generates highly accurate and stable microwaves that are transmitted to the JJA chip by an assembly of standard WR-12 waveguides for the excitation of the superconducting junctions.

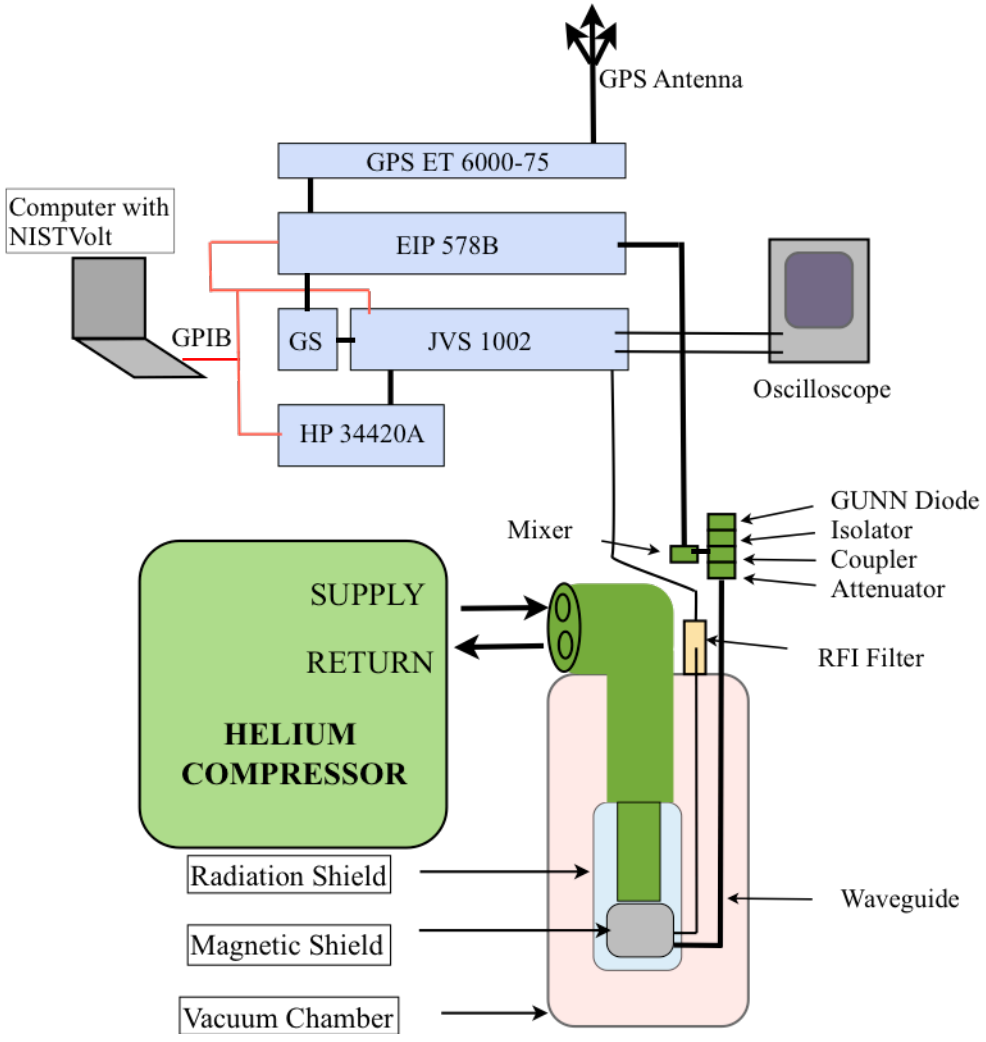


Figure 2.6: Diagrammatic representation of the assembled portable Josephson Voltage Standard System.

Another key component of the instrumentation assembly is the JVS1002 [51, 52] controller. Since the primary purpose of voltage standard system is to measure the terminal voltage at the JJA chip, the JVS system controller controls and automates the complete system. The JVS1002 is the main controller for the JVS system and is

connected to the system computer via the IEEE-488 port. The JVS1002 controller can be operated and controlled manually or by the NISTVolt [53] (trademark NIST) software installed in the system computer. Along with making crucial measurements required for the operation and conducting calibrations with the Josephson Voltage Standard system, the JVS1002 controller provides the bias current for the JJA chip and monitors the voltage at the JJA chip. The connecting wires from the JVS1002 controller to the JJA chip pass through RFI filters that eliminate any noise signals generated due to external factors.

A high performance digital nanovolt meter, HP 34420A, is connected to the JVS controller with an IEEE-488 interface. A set of cables providing the measurement of output voltage from the JJA chip exit the switching panel of the JVS1002 and provide the signal input for the digital voltmeter (DVM). Interface of the voltmeter with the NISTVolt software on the system computer provides the capability of controlling the DVM and obtaining the measurement data during the regular operation of the system as well as during the calibration process involving other equipment and/or other Josephson systems.

The rest of this dissertation is dedicated to discussing and presenting the in-depth research carried out during the development of each subsystem and presenting the results obtained from the UNC-Charlotte Josephson Junction Voltage Standard System.

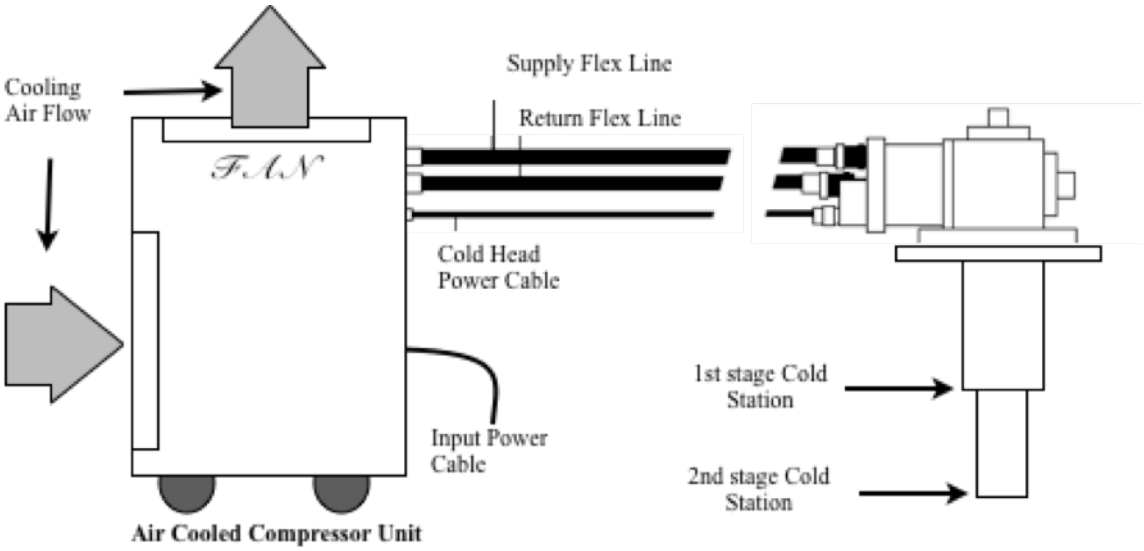
CHAPTER 3: THERMAL MANAGEMENT

The Josephson junction array based voltage standard system is a widely accepted dc voltage standard because of its stability and high accuracy of measurement. The generation of voltage, 1 V or 10 V, and the operation of the system are dependent on the temperature achieved by the JJA chip. The Josephson voltage standard systems currently used typically utilize liquid helium as the cryogen for cooling the JJA chip. The chip is securely mounted on a cryoprobe and the complete assembly is immersed in a liquid helium bath. The superconductor utilized for fabrication of the Josephson junctions are operated at a temperature close to the liquid helium temperature of 4.2 K. The use of liquid cryogen makes it logistically difficult to provide a transfer level voltage standard calibration system; so a portable JVS system is designed using closed cycle refrigeration system and the details of the design are discussed in this chapter.

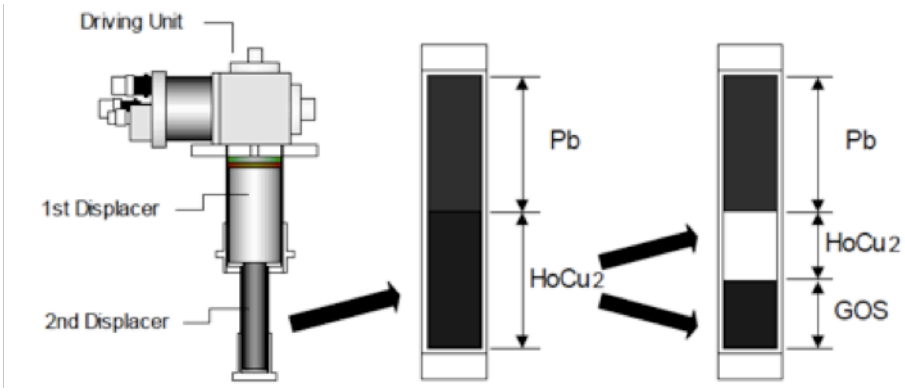
3.1 Cryocooling System

Commercially, there are different closed circuit refrigeration (CCR) systems available that can be built to customized specifications. The University of North Carolina at Charlotte Josephson Voltage Standard (UNCC-JVS) system utilizes a high efficiency closed cycle cryogenic refrigeration system to achieve an operating temperature in the vicinity of 4 K at the JJA chip surface. The complete cryocooler system was manufactured by Sumitomo Heavy Industries and consists of a Cold Head (RDK-415D), compressor unit (CSA-71A), helium flex lines and Cold Head power cables [45-47]. Figure

3.1 (a), provides a diagrammatic representation of the complete cryocooling system consisting of the air cooled compressor unit, the cold head, the helium flex lines and the power cables operating the cold head and Figure 3.1(b) shows the cross section of the second stage cold head displacer.



(a): Sumitomo Cryocooling system [45-47].



(b): Cross section of the Cryocooler Second stage regenerator [45-47].

Figure 3.1: Cryocooling System

The RDK-415D 4 K Cold Head is a two-stage Gifford-McMahon (GM) cycle cryo-refrigerator that produces a continuous closed-cycle refrigeration. Depending on the heat load imposed on the system, the cold head achieves temperatures of 25 K to 40 K at the first-stage cold station and 3.5 K to 4.2 K at the second-stage cold station [45-47]. As shown in Figure 3.1, the assembly of the cold head consists of three major components, namely the drive unit, the cylinder and the displacer generator assembly, which is located inside the cylinder. The second stage displacer consists of lead (Pb) spheres, which enable the 2nd stage to achieve temperature of around 10 K [45]. Further, magnetic rare earth regenerator material $HoCu_2$ (Holmium-Copper$_2$) is used in the 2nd stage displacer to achieve an operating temperature of 4 K [54, 55]. Another regenerator material, Gd_2O_2S (Gadolinium Oxide Sulfide, GOS) is also used; because of its high volumetric specific heat a lower temperature is achieved at the cold head and allows significantly better cooling capacity to achieve an operating temperature of 4 K [45]. The use of rare earth regenerator material enables the Cold Head to have a second stage refrigeration capacity of 1.5 W at 4.2 K.

The cold head of the cryocooler is connected to the compressor unit with helium gas supply connectors. The compressor unit controls the high-pressure flow of helium gas to the cold head cylinder. During the operation cycle, the high-pressure (1.65 MPa at 20° C) helium gas passes into the displacer-regenerator assembly, comes out through the displacer-regenerator assembly to the crank case through the motor housing and finally returns to the compressor unit through the helium gas return connector [45]. The helium gas expansion in the displacer-regenerator assembly provides the cooling condition for first and second-stage cold stations. For further details on the operation of the cryocooler,

the reader should refer to references on the Gifford-McMahon (GM) refrigeration cycle and/or the Sumitomo Cryocooler operation manual [45-47]. The Sumitomo system required either 20 meter flex lines or 6 meter lines combined with buffer tanks. In our case, the 6 m flex lines were used with buffer tanks to facilitate packaging the unit in the instrumentation cabinet; the supply and return buffer tanks are inserted between the compressor unit and the flex lines. Figure 3.2 shows a diagrammatic representation of the complete system assembly.

3.2 Vacuum System

The complete cryocooling system consists of commercially available components that can be repaired or replaced as needed. For achieving the temperature of 4 K at the cold head of the cryocooler the two-stages of the cryocooler must be enclosed in a vacuum chamber. The vacuum chamber is created by machining an aluminum cylinder to surround the two stages of the cryocooler and is attached to the base of the motor of the cryocooler, as shown in Figure 3.2. An Alcatel mechanical vacuum pump is used to draw down the vacuum. A fixture is created across the vacuum chamber so that the chamber and the cryocooler can stand independently. For the operation of the cryocooler, first a high vacuum of near 1 x 10^{-3} Torr is achieved in the chamber. The high vacuum environment surrounding the first and second stages of the cryocooler helps to ensure a low heat load at the cold head by nearly eliminating losses due to convection, thereby improving cryocooler efficiency. The vacuum inside the chamber is monitored by a pressure sensor connected to the vacuum line and is displayed on a pressure gage for convenience of the operator. Once the chamber reaches a vacuum of 10 mT, the cryocooler is turned on to begin the cool down cycle. The cooling of the cold head helps

draw the vacuum down further by cryo-pumping. Silicon diode temperature sensors attached to the 1st and 2nd stage of the cryocooler monitor temperature at the cold head during cool down, which takes approximately 120 to 150 min. Figure 3.2, provides a diagrammatic representation of the assembled cryogenic and vacuum system.

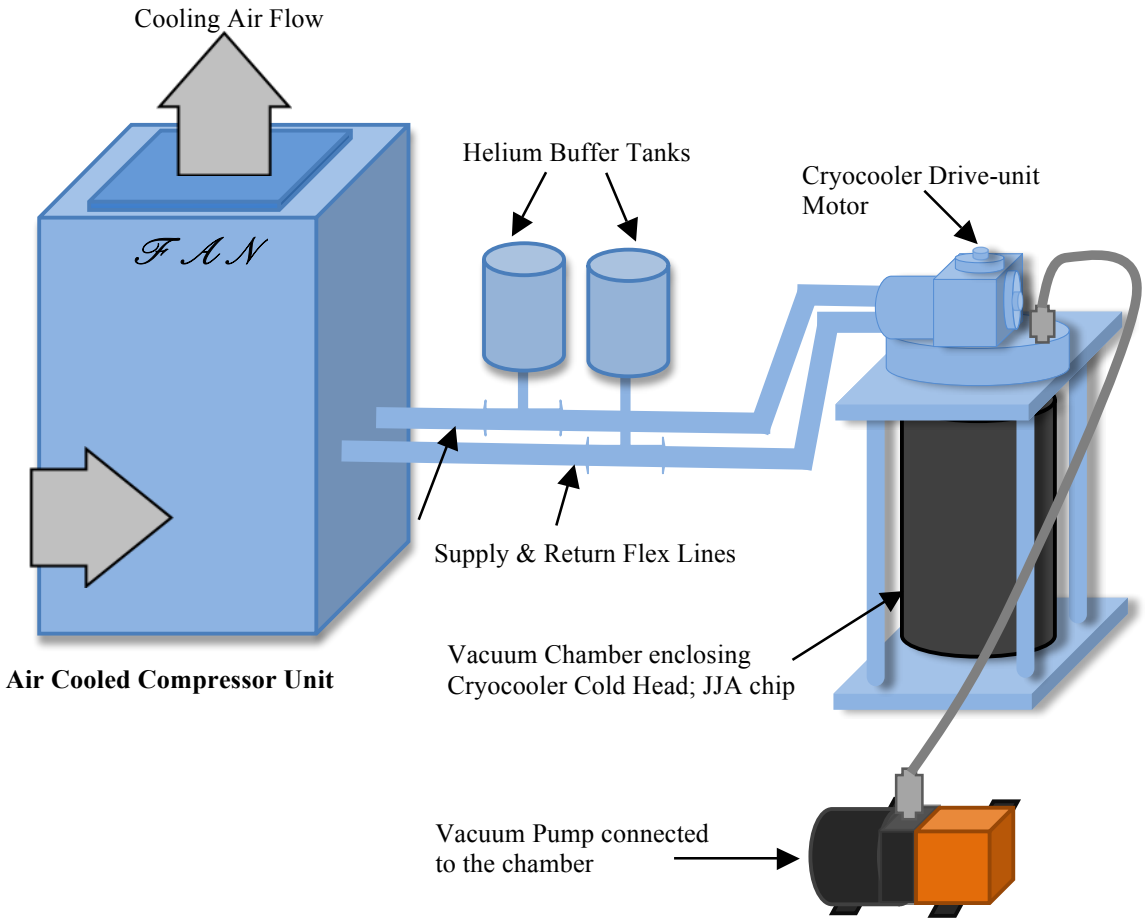


Figure 3.2: Diagrammatic representation of the cryocooling and vacuum system.

The complete voltage standard system needs to be built in such a way that it can be rack mounted in the standard cabinet of size 56 x 82 x 195 cm. The components of the closed circuit cryocooling system and the vacuum system require careful packaging to fit into the cabinet. The compressor unit (CSA-71A) made by Sumitomo Ltd. has physical

dimensions larger than the standard rack. So, in order to make sure that all the components of the system fit properly in the rack, the compressor unit was disassembled and the internal components, like the helium gas storage tank, filter, compressor capsule, adsorber, radiator, cooling fan, switches, electronic control box, etc., were restructured and fitted to a newly designed enclosure for the compressor unit. The airflow of the compressor unit was rearranged to provide optimal cooling within the cabinet. The flow of gas and oil in the compressor unit was taken into consideration to ascertain proper and safe operation of the unit. The original design of the CSA-71A unit had the air intake on the front face of the unit and the air discharge including the fan located on the top face of the unit. In the new design of the compressor unit, the air inlet is positioned in the front of the unit and the air discharge unit, including the fan, is moved to the back of the compressor unit. Figure 3.3 shows the assembled compressor unit and the vacuum system mounted on the standard rack. The bottom portion of the rack is physically separated from the top of the rack using an aluminum plate that also acts as a base for mounting the vacuum chamber. The vacuum pump, helium buffer tanks and the fixture holding the cryocooler and the vacuum chamber are positioned on top of the aluminum plate. The six-meter long helium flex supply and return lines are securely fastened to the sides of the rack. These lines, coupled with the buffer tanks, allow limited compliance in the system for dynamics, preventing the option of replacing the flex lines with hard fittings. The vacuum chamber and the cryocooler are mounted on the separating aluminum plate and sit on top of a spring-damper suspension system. The suspension system provides shock-absorbing capabilities to the vacuum chamber, which holds the highly sensitive JJA chip.

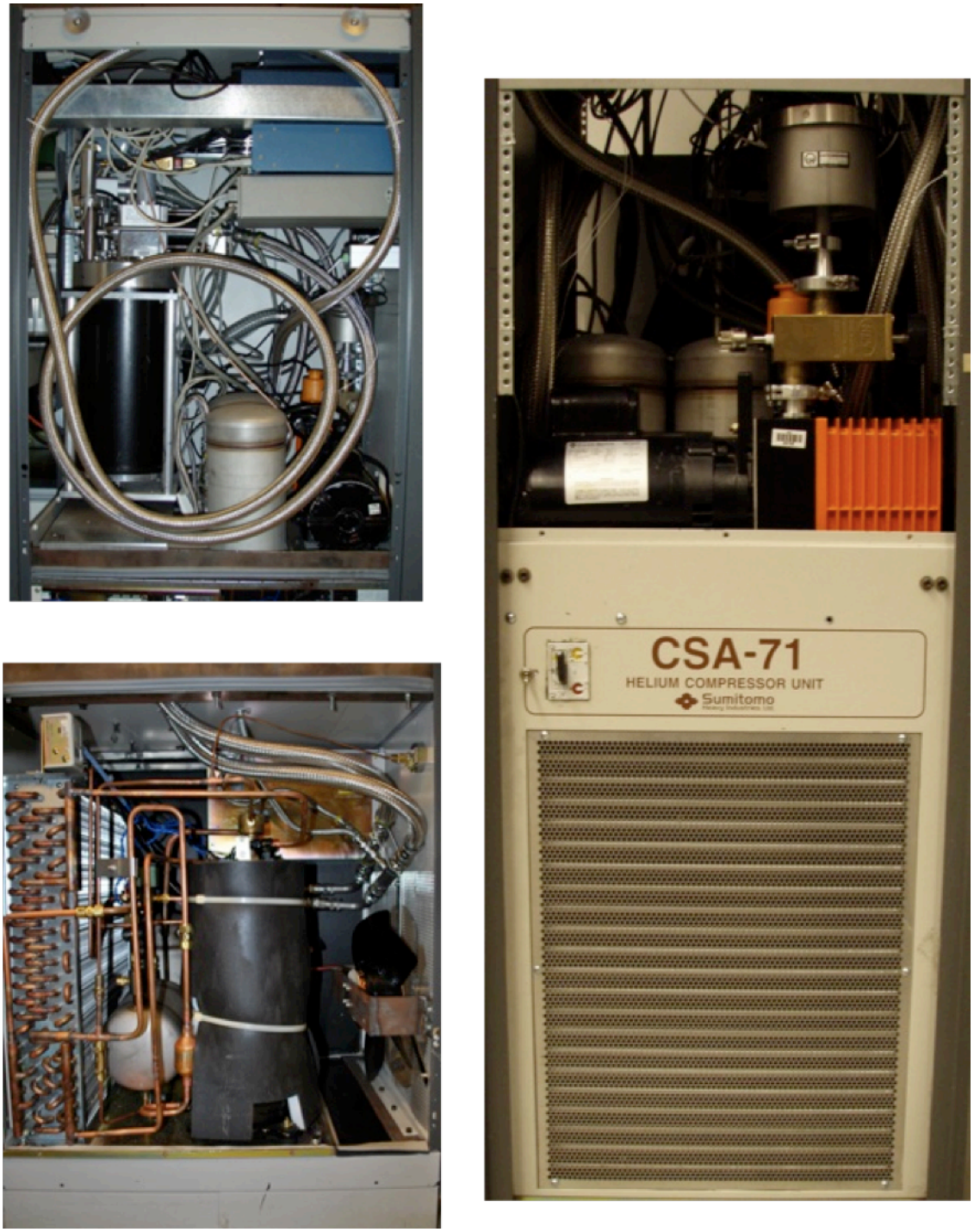


Figure 3.3: Redesigned compressor unit, cryocooler assembly and the vacuum system mounted on a standard rack mount.

3.3 Mounting of Josephson Junction Array chip

The complete assembled cryocooling system has the capability to cool the second-stage cold station of the cryocooler in the range of 3.5 K to 4.2 K, depending on the heat load of the system. For the Josephson Junction Array (JJA) chip to operate and provide the specified performance, it needs to be cooled down to a temperature below the critical temperature of niobium (9.2 K). Once the system was assembled, it was tested using the procedures discussed earlier and a temperature of 3.5 K was experimentally achieved and measured on the cold head of the cryocooler using silicon diode temperature sensors.

A fixture that would allow the chip to establish an efficient thermal conduction path to the cold head was required in order to cool the JJA chip to the operating temperature. The fixture was also necessary to securely hold the chip and restrict motion of the chip in any direction. Figure 3.4 shows images of the JJA chip mounting fixture (fabricated out of Oxygen Free High Conductivity (OFHC) copper) and other critical components. The JJA chip sits on the middle pedestal of the chip-mount and a piece of FR-4 surrounds the chip, as seen in Figure 3.4 (a). The pedestal of the JJA chip is machined to such a thickness that the FR-4 surround creates a raised wall surrounding the chip, hence completely restricting any lateral motion of the chip. The electrical connections for providing the bias current and measurement of the voltage are established using copper-beryllium (Cu-Be) fingers fabricated on the FR-4 fingerboard, as shown in Figure 3.4 (d) and (e). The FR-4 fingerboard must be maintained at a controlled height to ensure sufficient but limited force on the chip to prevent damage. Also, it is required to have the microwave power delivered to the Josephson junctions on the chip. The fixture is designed in such a way that the opening on the microwave waveguide delivers the

microwaves to the fin-line antenna fabricated on the JJA chip, which is essential for the actuation of junctions on the chip. The positioning of the chip with respect to the waveguide opening can be seen in Figure 3.4 (b).

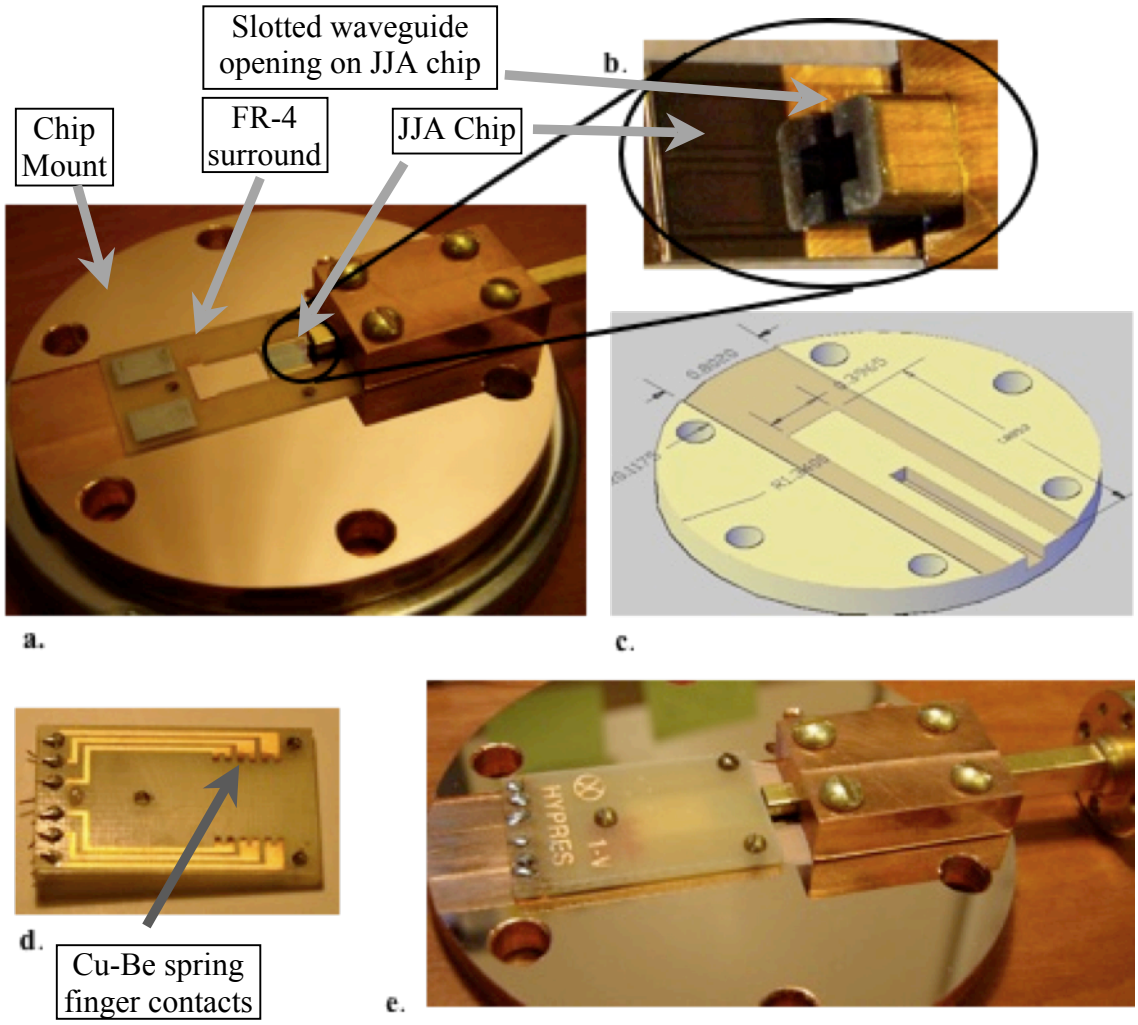


Figure 3.4: (a) Image of chip mount with the JJA chip and the FR4 surround; (b) position of waveguide and JJA chip; (c) dimensional representation of chip mount; (d) FR4 circuit board with Cu-Be spring finger contacts, and (e) complete assembly on chip mount.

The OFHC copper chip mount sits on a set of six copper posts and is firmly anchored to the cold head of the cryocooler using brass bolts. The copper posts help in holding the magnetic shields that create an envelope of low magnetic flux region around the JJA

chip; the use of these magnetic shields will be explained during the discussion on the design of magnetic shields in Chapter 5. Figure 3.5 shows the complete assembly of the JJA chip mount attached to the cold head of the 4 K-second stage of the cryocooler. The magnetic shields are eliminated from this picture for clarity. The chip mount has a silicon

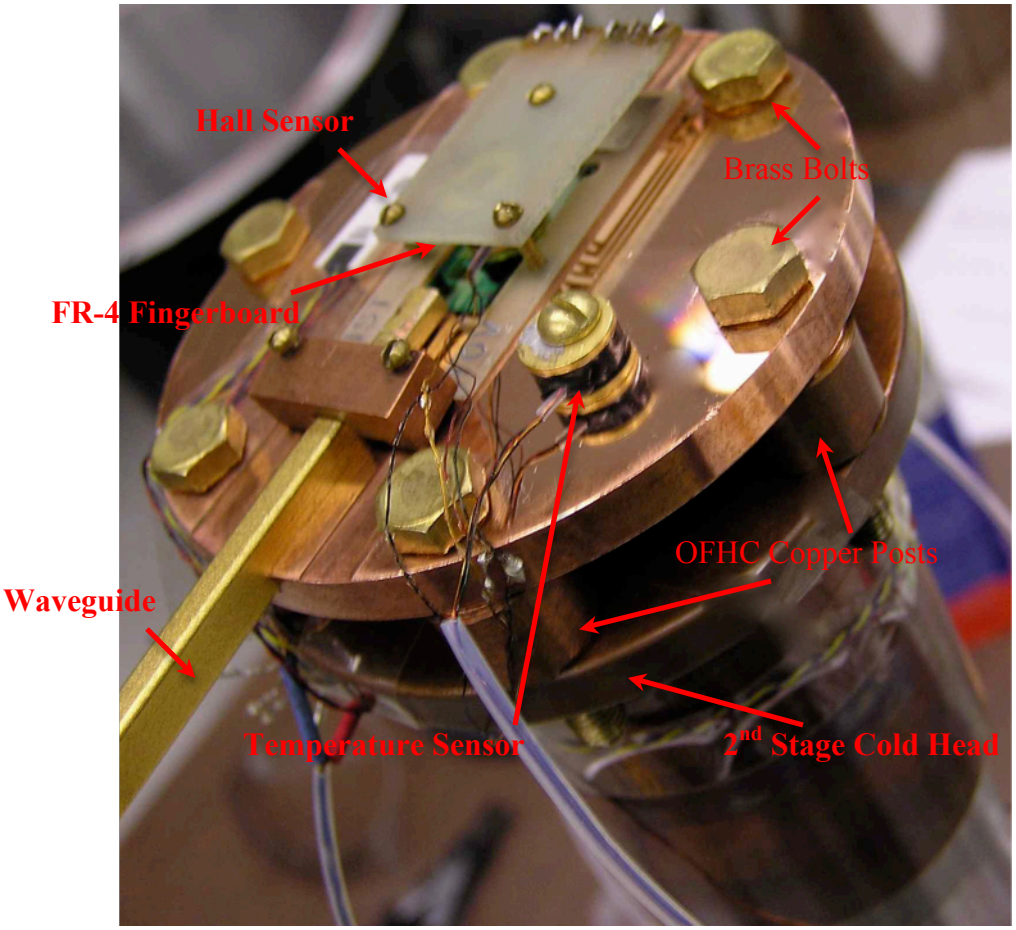


Figure 3.5: Image of the chip mount assembly attached to the 2nd stage cold head of the cryocooler.

diode temperature sensor attached to it for the measurement of surface temperature as well as a Hall sensor for measuring the magnetic fields in the vicinity of the JJA chip. During operation of the Josephson voltage standard, heat is produced from the incident microwaves and any thermal paths such as sensor wires that contact the outside of the

chamber. The 1 volt JJA chip consists of around 2000 superconducting junctions (20,000 for a 10 V chip) that need to be maintained below the critical temperature of the superconductor. As the junction reaches a temperature higher than, or close to, the critical temperature of niobium it looses the property of superconduction. Hence, the rate of cooling of the chip should be greater than the rate of heat produced during the operation. The 'heat-lift' of the system is calculated considering all the sources introducing heat [79]. As shown in Figure 3.4 and 3.5, the Cu-Be (Copper Beryllium) fingers on the circuit board establish a physical contact with the contact pads on the JJA chip and on the other side of the fingerboard the Cu-Be fingers are soldered to six copper wires (AWG-32). This set of six wires connect the JJA chip to the system controller and provide the bias current to the chip while measuring voltage across the circuit. One end of these copper wires is connected to the chip and the other end is soldered to the connector, which leads them outside the vacuum chamber. Having one end of the wire at the chip and the other end at room temperature provides a direct thermal conduction path from the chip to room temperature, approximately 295 K, and adds to the heat load at the JJA chip. To reduce the temperature gradient along the length of the wires, all the copper wires and the sensor cables are thermally anchored to the body of the cryocooler at the first stage, at 50 K, and at the second stage at 4 K.

3.4 Thermal Radiation Shield

Once the thermal convection and conduction was engineered, the next step was to reduce thermal radiation load. In contrast to the heat transfer by conduction or convection, we know that the heat transfer by thermal radiation does not require the presence of any medium or matter. In case of the JVS system, the operating temperature

is close to 4 K, which is nearly 290 K lower than the room temperature. The chip mount and the cryocooler cold head, operating at 4 K, are completely exposed to the inner surface of the vacuum chamber, which is maintained at room temperature. Radiation heating is a function of temperature difference raised to the fourth power as shown in Equation 3.1, and is therefore a significant source of heat load to the system.

$$q \propto \sigma(T_1^4 - T_2^4) \tag{3.1}$$

In this equation, q is the net rate of radiation transfer, σ is the Stefan-Boltzmann constant and T_1 and T_2 are the two operating temperatures.

For a system that is highly sensitive to the operating temperature, a difference of 290 K destabilizes the system due to radiation heating. A radiation shield was therefore fabricated and used to reduce the net radiation transfer between the two surfaces. The radiation shield was designed in such a way that it can be securely bolted to the first stage of the cryocooler. By thermally anchoring the radiation shield at the first stage, an operating temperature of 45 K was obtained at the shield surface. Reducing the exposure temperature of the chip mount from 295 K to 45 K, reduces the heat load by a factor of more than 1800, which is a significant amount.

Once the radiation shield was put into place and thermally anchored to the first stage, the temperature distribution at the surface of the shield was measured using temperature sensors. Temperatures were taken at various locations on the radiation shield and were verified to be 42 ± 1 K over the surface.

Figure 3.6 shows the final design of the radiation shield with the base plate fastened to the first stage of the cryocooler with brass bolts. One very important factor to be considered while designing the radiation shield is that every single component connected

to the chip mount at the second stage should be enclosed inside the radiation shield. In order to reduce the heat load at the chip mount, the waveguide assembly used is a combination of the WR-12 rigid and flexible waveguides. The portion of waveguide attached to the outside of the vacuum chamber is flexible waveguide, made of thermally dielectric material. This creates a disjoint in the thermal conduction path to the chip mount, providing isolation from the outside environment. The remainder of the waveguide is cooled through its thermal contact with the chip mount. In one of the previous radiation shield designs, the waveguide assembly, seen in Figure 3.6, was outside the radiation shield and created tremendous amount of heat load at the chip mount surface. The heating of the waveguide was much higher than the cooling capacity of the cold head at 4 K. After several experimental runs the temperature distribution shown in Figure 3.6 was observed at the waveguide surface.

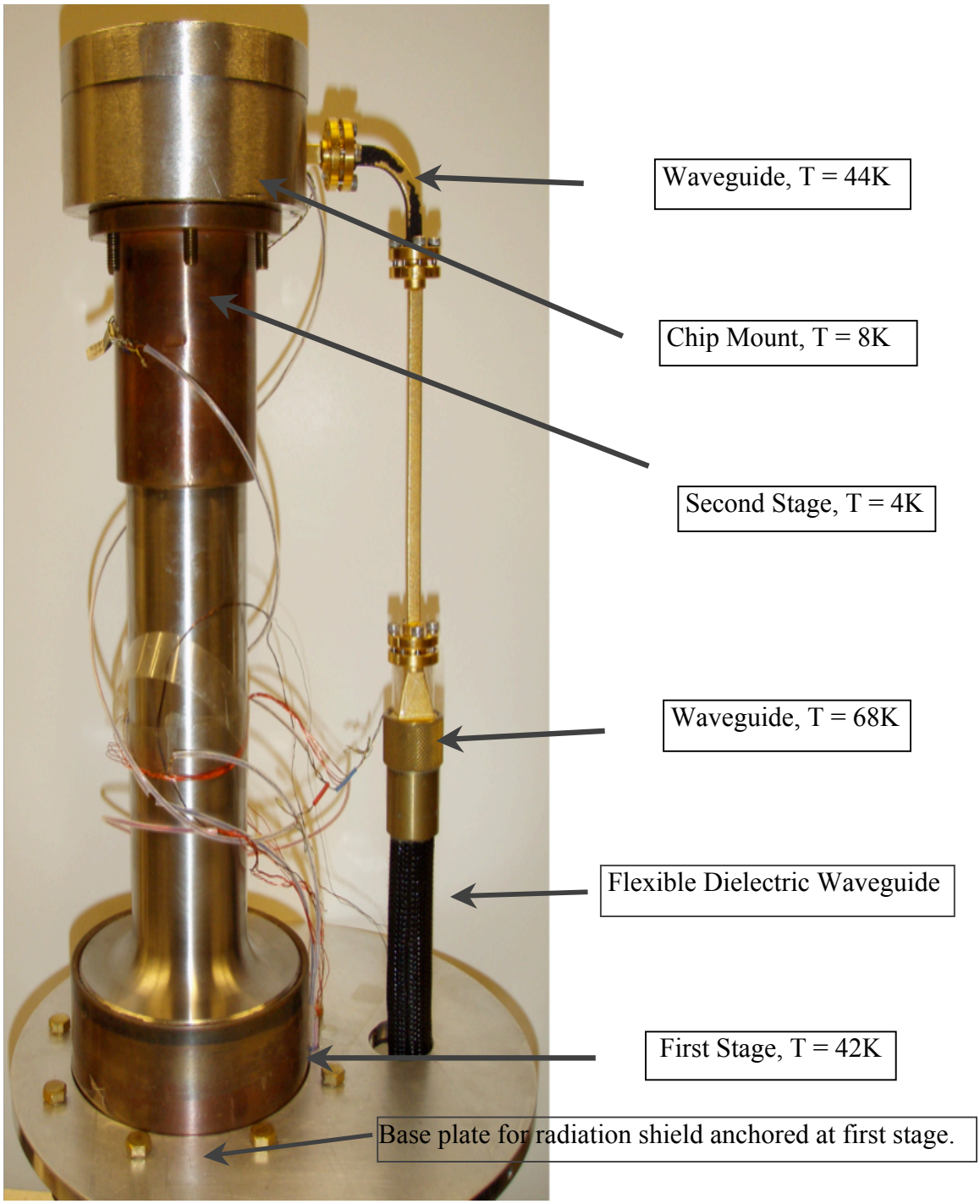


Figure 3.6: Temperature distribution on the waveguide.

3.5 Conclusion

In this chapter we presented the design of a compact closed-cycle refrigerator (CCR) system and created a prototype for experimentation. By redesigning the compressor unit for the system and building the required vacuum system to support the operation of the cryocooling system, the required temperatures were obtained while meeting the packaging requirements specified by the US Army. This system has the capability of cooling the JJA chip down to 4 K and maintaining it at that temperature during the course of calibration cycles. Thus, the required goal of putting together a CCR based cryocooling system that would achieve the operating temperature of 4 K was successfully achieved.

The main difference between a liquid helium Dewar based cooling system and a closed-cycle refrigeration system for the JVS system is the mode of heat transfer for cooling. In case of the liquid helium Dewar based system, the JJA chip is mounted on a cryoprobe and immersed in liquid helium bath. In this case, all the surfaces of the JJA chip come in direct contact with liquid helium and the heat transfer takes place via thermal convection; till the liquid helium level is maintained in such a way that the JJA chip is completely immersed, the chip will attain and maintain a temperature of 4.2 K. On the other hand, a CCR based cryocooling system completely relies on thermal conduction between the JJA chip and the chip mount for cooling the chip. In the CCR based system, any thermal path that can add to the head load at the cold head has to be eliminated. The heat load is added to the cold head from all the modes of thermal transportation.

In order to reduce heating due to convection, a high vacuum of at least 10^{-3} Torr (preferably 10^{-6}) must be achieved and maintained during operation. The presence of

vacuum allows the cold head to achieve its operational temperature of 4 K and eliminates any contamination due to presence of environmental molecules. All the temporary joints to the chamber must be sealed using high vacuum o-rings (preferably Viton®). The o-ring grooves must be thoroughly cleaned and none of the components inside the vacuum chamber must ever be touched by bare hands; as this introduces oils and other contaminants. Another mode of thermal transfer is radiation; since the outside chamber is exposed to room temperature, every component inside the chamber is exposed to thermal radiation. The components that fall in the line-of-sight of the chamber walls are constantly exposed to radiation from a source at nearly 295 K. Exposure to this kind of heat radiation adds a lot of heat load and can easily stop the cold head from reaching a temperature of 4.2 K. To reduce the affect of thermal radiation heating, radiation shields must be created to surround the components and the shields must be thermally anchored to different cold head stages for thermal cool down.

The temperature sensors, magnetic field sensor and the JJA chip are electrically connected to the controllers and electronics measurement devices outside the vacuum chamber. The wires connecting the sensors and the chip to the connectors on the outside chamber walls are at a temperature of close to 4 K on one end and at room temperature (295 K) on the other end. This provides a direct thermal path to the cold head by conduction and the heat load induced is enough to disrupt the delicate temperature balance at the JJA chip mount. Also, the exposure of these wires to a temperature difference of nearly 290 K introduces electrical noise into the system. To avoid the heat gradient along the length of these wires, they are thermally anchored to the two stages of the cryocooler and along the body of the cryocooler tube by heat sinking the wires using

GE varnish 7031 (VGE-7031). All the other metal-to-metal contacts are lightly coated with a low temperature thermal grease (Apiezon N®) in order to increase the thermal contact conductance of the mating surfaces. This chapter discussed the thermal management of the system presenting in-depth analysis of conduction cooling of the JJA chip and design of the CCR system. In the next chapter, a detailed analysis of the thermal contact conductance problem is addressed, where, the dependence of heat flow across the interfacing surface of the JJA chip and the cryocooler cold head was studied and new mounting techniques were developed and tested.

CHAPTER 4: THERMAL CONTACT CONDUCTANCE

Whenever there is a physical interaction between two interfacing surfaces, the surface parameters such as roughness, flatness, waviness, etc. come into discussion. Among many other properties, the thermal behavior of a junction of two interfacing solids is highly dependent upon the surface parameters. The rate of flow of heat across a junction of two surfaces is defined by a parameter known as the Thermal Contact Conductance (TCC). The mechanical interface between the Josephson Junction Array (JJA) chip and the OFHC copper chip-mount is responsible for cooling the chip to cryogenic temperatures. The magnitude of thermal contact conductance is dependent on parameters such as the thermal properties of the interfacing materials, contact pressure, interfacing materials, surface geometries, etc [56-69]. Thus, it is very important to create a model for detailed study of the contact mechanics to predict the thermal contact conductance. This chapter describes an analysis that was conducted to analyze the thermal characteristics of the chip mount and its affects on the operational cryogenic temperature for the JJA chip.

4.1 Introduction

The JJA chip consists of superconducting junctions made up of Niobium, which has a critical temperature of 9.2 K [70]. For stable operation of the JJA chip, it has to be maintained at a temperature close to 4.2 K [7]. Earlier, liquid helium was used to cool the JJA chip to the required cryogenic temperature; the complete assembly of fixture along with the chip would be gradually dipped in the liquid helium bath. Once the chip is

immersed in the bath it achieves the temperature of 4.2 K and stays at that temperature till the level of liquid helium is maintained in the Dewar. Since the complete volume of the chip is dipped in helium, it is easy to achieve the operational temperature and maintain it.

On the contrary, the CCR based cooling system completely relies on thermal conduction to cool the JJA chip. As explained in the previous chapter, the chip is kept in an airtight chamber and maintained under a vacuum of $1x10^{-3}$ Torr; this means that there is no heat transfer by means of convection. The design of fixture utilized to hold the JJA chip is such that the chip sits on the OFHC copper chip mount, is surrounded by a FR-4 surround on the sides, to prevent any lateral movement of the chip, and is covered with a FR-4 fingerboard on top; Figure 3.5 showed the picture and discussed the design of fixture assembly. FR-4 is a thermal insulator and hence does not offer any conduction path for cooling of the chip. The copper chip mount, physically attached to the second stage of the cryocooler, allows it to reach the lowest temperature of 3.5 K. Since, thermal conduction is the only way of cooling the chip, it is necessary to maximize the thermal contact conductance at the junction of the JJA chip and the OFHC cooper chip-mount.

Contact cooling is the only method of heat removal from the JJA chip during the operation of the system. At the macroscopic level, there exists a good thermal contact between the JJA chip and the copper surface, but experimental results show a lack of required thermal contact conductance between the two surfaces. To reduce the thermal resistance between the surfaces different possibilities were looked into and some options were experimented with. A detailed analysis of the thermal contact conductance was

carried out and a solution to achieving the required operational temperature was found and experimentally achieved.

In order to model the heat transfer phenomenon, contact between the surfaces has to be characterized in terms of flatness, waviness and the roughness of the surfaces. The influence of these parameters on thermal conductance is very difficult to model because of the complexities involved in creating an exact representation of these parameters in three-dimensional topography. Even though the complete modeling of the contact phenomenon would be very complex, it is essential to establish a predictive model that would consist of the different factors on which the thermal contact conductance depends. In this chapter we concentrate on achieving a practical solution that experimentally allowed us to reach the critical temperature and maintain it during the complete operational cycle.

4.2 Thermal Contact Conductance

The surface parameters of a solid material can be deceiving if observed only at the macroscopic level. When investigated at the micro-scale, it is reveled that the contact phenomenon of the two interfacing surfaces occurs only at a few discrete contact points. These few contact points are the main cause of a high thermal resistance. The constriction of the heat flux to the spots of real contact creates barrier to the heat flow, hence causing the high thermal resistance. The actual physical contact is imperfect and the heat transfer area is just a small fraction of the apparently contacting cross-sectional surface area. It can be seen in Figure 4.1 that the surface, which appears to have a very low roughness value at a macroscopic level, revels to be very rough when looked at the microscopic level. The figure shows that the heat flow lines are constricted to the few good contact

points, hence, producing higher heat flow densities at the contact points. These in turn require much higher driving potentials.

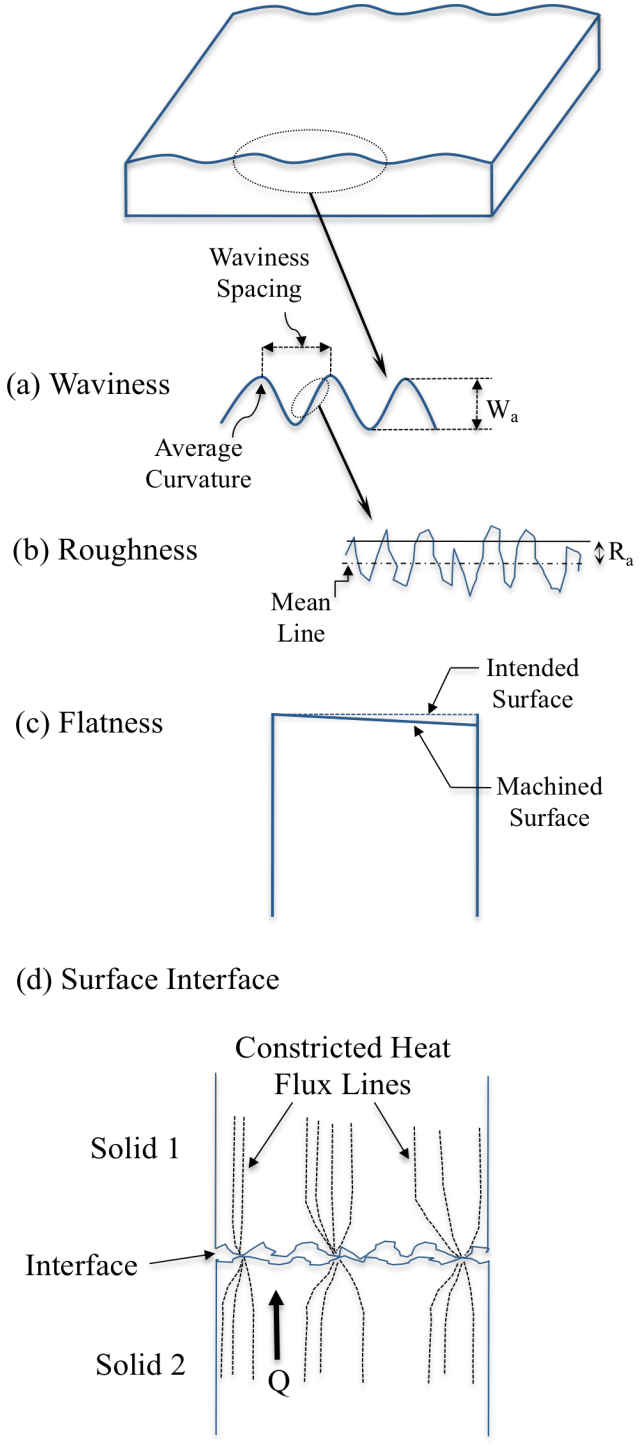


Figure 4.1: Surface characteristics of contacting surfaces.

The thermal contact conductance h, can be explained by the equation,

$$h = \frac{q}{\Delta T}, \tag{4.1}$$

where, q is the heat flux across the surface and T is the temperature drop across the contacting surfaces. Further, the heat flux q, is defined as follows,

$$q = \frac{d}{dA}\left(\frac{dQ}{dt}\right) \tag{4.2}$$

where, Q is the heat flow rate through the contact and A is the actual area of contact for the thermal resistance.

The value of thermal conductance h, varies substantially dependent upon several parameters such as, the temperature, macro and micro parameters of the surface geometry, contacting materials, pressure at the contacting surfaces, presence of interfacial materials, etc. Our model looks into the thermal contact conductance between the bottom surface of the JJA chip and the top surface of the OFHC copper chip mount considering the significant parameters in detail.

The JJA chip is fabricated on a silicon substrate and the chip mount is machined out of an OFHC copper workpiece. The two materials considered for our study are hence known and narrows the scope of work to finding the thermal conductance between copper and silicon. The chip mount designed for holding the chip was fabricated by conventional machining of a single OFHC copper workpiece. The machining was done on a Makino Delta-A55 CNC and the final machined chip mount had an interfacing surface with a high level of flatness.

4.3 Mathematical Model and Problem Definition

Based on the equations discussed earlier, an approximate value for the thermal contact conductance between the OFHC copper surface and the silicon chip can be calculated. The footprint of the silicon chip is considered for the contact surface area between the two surfaces. Since the chip mount is in thermal contact with the coldhead of the CCR system, analysis reveals that attaining a temperature that us equal to that of the cold head (~3.5 K) at the chip mount should be possible. Experimentally, temperature sensors attached to the top of the surface confirmed the results by attaining a temperature of 3.5 K.

The heat flux, q, across the contacting surfaces is dependent on the surface characteristics and the resistance offered to the flow of heat across the junction, is known as the thermal contact resistance, R_c, and is defined as,

$$R_c = \frac{\Delta T}{Q} \tag{4.3}$$

It is very difficult to calculate the exact value of the heat flow across the junction because of the various unknown parameters introduced due to the consideration of surface characteristics. The heat flow equation,

$$Q = h_c . A \Delta T \tag{4.4}$$

where, Q, is the heat flow rate across the junction, shows the dependence of heat flow rate on the actual surface area of the contacting bodies.

Mathematical calculations suggest that for the contacting surface area of the JJA chip to the chip mount, the chip should be able to attain the temperature of up to or lower than 4.2 K. The operation of JJA chip is highly dependent upon the temperature attained by the superconducting junctions on the chip. As soon as the superconducting material,

niobium in this case, is cooled down below its critical temperature, a small amount of current starts flowing across the Josephson junctions. This transition to a superconducting phase can be observed by the display of a characteristic I-V curve, Figure 4.2. The operation of Josephson junction has been discussed in detail in Chapter 2. The I-V curve can be used to estimate the temperature dependent leakage current in the array. If this value is higher than the operational value, the array becomes too unstable to operate. Further, if the temperature is even higher than that, the I-V curve is not displayed at all.

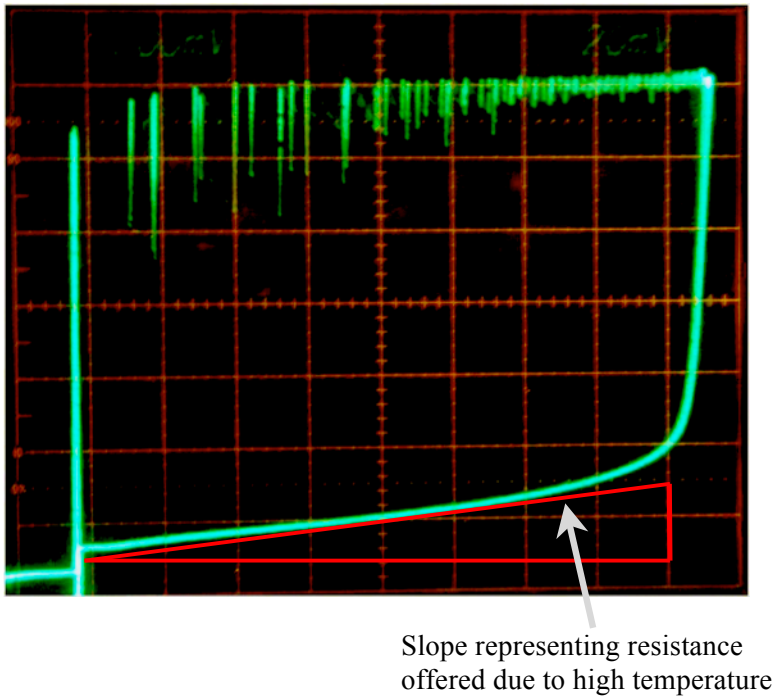


Figure 4.2: I-V curve displaying current loss due to high temperature.

The experimental results showed a lack of proper I-V curve, which was a clear indication that the JJA chip was not operating at the required temperature. On detailed inspection it was observed that the vast discrepancy between the experimentally obtained and the calculated temperature at the chip was due to the surface characteristics causing a

lack of sufficient contact between the two interfacing surfaces. The interface resistance is mainly caused due to the unevenness of the actual surfaces. In actuality, the contact between the surfaces is imperfect and they touch only at a few discrete points. Thus, the heat transfer between the two contacting surfaces occurs only at these few physically contacting points. The JJA chip mount was very precisely manufactured by high speed machining from an OFHC copper work piece. The contacting surface of this mount was measured to have a very high flatness value. Figure 4.3 is a picture representing the surface of this chip mount. It appears to have a good surface finish at the macroscopic level, but the same surface, when observed under a microscope, appeared to have a very uneven profile. The image at a higher magnification reveals that the area of contact between the two surfaces is considerably lesser than the numbers assumed during modeling.

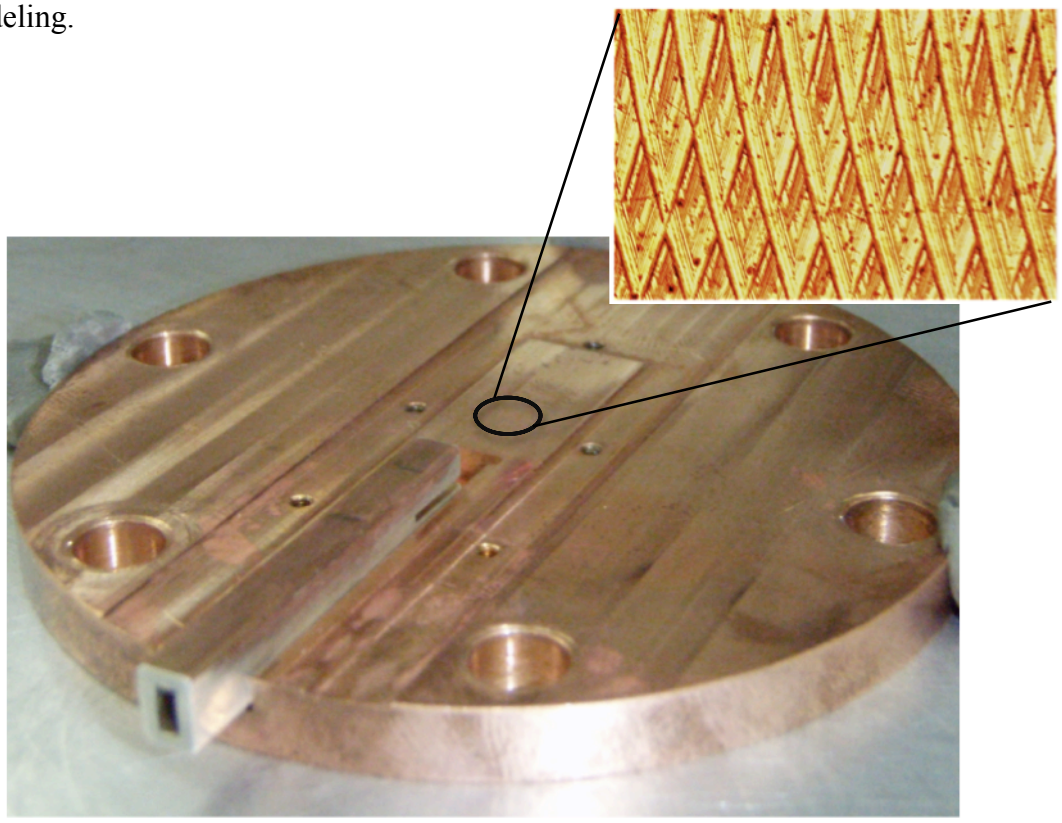


Figure 4.3: Optical microscope image of the chip mount showing machining tool marks.

In the higher magnification view of the surface, the machining tool marks appear to form ridges on the surface. When the JJA chip is placed on top of this surface, the chip is actually in contact with only the highest peak points of these tool marks, which significantly reduces the surface area of contact. Further, the measurement of profile of this surface area revels that not all the peak points on the surface are of same height. Figure 4.4 is a profile plot obtained from an Alpha Step contact profilometer measuring a span of approximately 500 μm. The measurements were made at different locations over the surface and indicated nearly the same nature of profile.

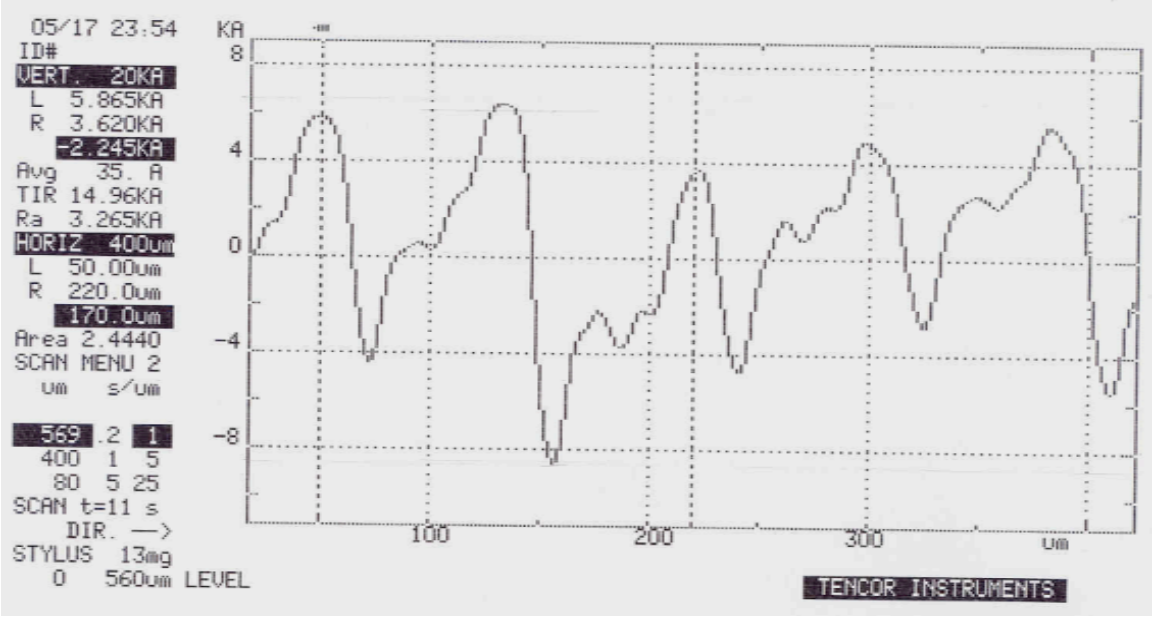


Figure 4.4: Surface profilometer plot of a conventional machined surface.

The appearance of random high peaks further reduces the contact area between the JJA chip and the chip mount surface. The drastic reduction of contact area, as compared to the assumed surface area, is clearly responsible for lack of attainment of the operational temperature at the superconducting Josephson junctions. Since, in the CCR

based cooling system, conduction is the only way of extracting heat from the JJA chip, it was necessary to explore the different methods of increasing the contact area between the two surfaces to achieve the required temperature. The next section presents the different options considered during this study and discusses the results for each method.

4.4 Conceptual Design and Approach

In the study of thermal contact conductance, for a set of known materials, the most significant parameter is the actual area of contact between the interfacing materials. There have been a lot of studies and research conducted in finding different ways of increasing the thermal contact conductance and one of the most common methods adopted is by applying pressure on the contacting materials [56-60]. Another very effective approach is by using an interstitial material at the contact interface [61, 63, 67, 69]. The use of a high thermal conductivity interstitial material provides an alternate path for heat flow between the two surfaces. There are different kinds of materials used based on the requirement of the situation. In this section a brief discussion is presented about the various methods considered and adopted during this research.

4.4.1 Application of Pressure

The measurement of thermal contact conductance is of high interest for researchers and engineers from the point of view of increasing the heat flow [56-61]. The values of thermal contact conductance have been derived based on different mathematical models and also some experimental models. Nearly all of the studies and publications state a relationship between the applied pressure at the junction and the thermal conductance or at least considers the applied pressure to be a significant part of the model [56-69]. As it is known, that there is a considerable reduction of the value of thermal contact conductance

due to the asperities of contacting surfaces [56, 58, 60, 64]; application of pressure at the junction tends to increases the contact area by elastically or plastically deforming the asperities, depending upon the mechanical properties of the materials involved. Since decades, researchers have constantly worked and created models and carried out experiments to observe and measure the dependence of contact conductance on the application of pressure. The dependence of pressure in increasing the heat flow across an interfacing junction is well researched and understood.

Calculation of load at the end of Be-Cu fingers as a cantilever beam:

The thermal contact conductance between two interfacing surfaces is highly dependent upon the contact pressure at the junction. Numerous studies have been carried out based on calculations and experiments that revel the high dependence of applied pressure to the performance of the interface [58-62]. As pressure is applied to the interfacing junction the asperities related to the contacting surfaces tend to change physically. The contact conductance of the junction can change either due to plastic or elastic deformation of the asperities. In either case, deforming the asperities at the junction increases the area of contact for the two surfaces that were previously touching each other only at a limited number of discrete points. The increase in thermal contact conductance is a clear indicative of dependence on the contact pressure.

In the model considered here, the change in thermal contact conductance of the interfacing surface between the silicon JJA chip and the OFHC copper chip mount due to the applied pressure at the junction is restricted by the material properties of silicon. Silicon being a very fragile material restricts the amount of pressure applied at the junction. The design of the JJA chip holder is such that the only pressure at the interface

is due to the weight of the chip and the pressure applied by the six beryllium-copper contacting fingers. The Be-Cu fingers are fabricated in such a way that they act like cantilevers with a preexisting deflection. The elastic properties of Be-Cu allow it to act like a spring pressing against the contact pads on the JJA chip, thus providing good electrical contact. Six of these Be-Cu fingers help in pressing the JJA chip against the chip mount surface. The FR-4 circuit board with the Be-Cu circuit is pressed against another piece of FR-4 that surround the JJA chip. Figure 4.5 shows the model considered

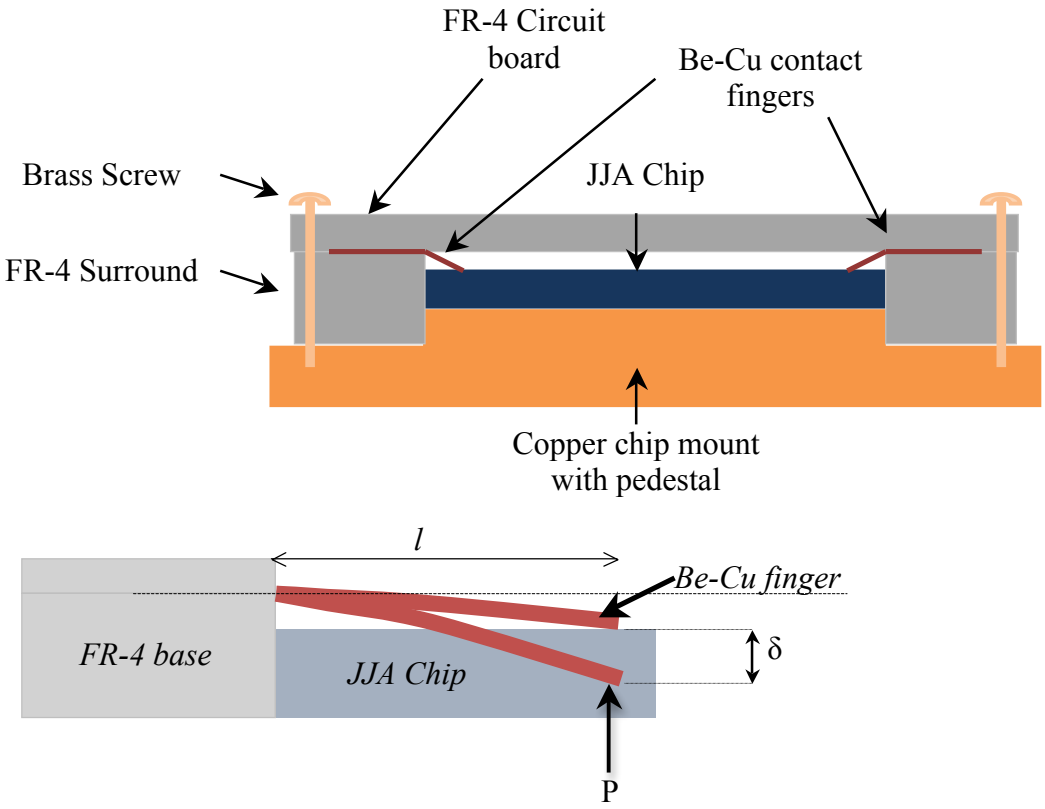


Figure 4.5: Modeling of Be-Cu finger as a cantilever beam.

for calculating the equivalent load at the tip of Be-Cu finger. The contacting surface of the two FR-4 pieces allows the Be-Cu finger to act like a cantilever beam. The measured dimensions of the Be-Cu finger are shown in the figure. If we define the default position of the Be-Cu finger as the unloaded beam and the position at the which the fingers

contact the JJA chip as being the loaded condition, the amount of load required to cause the deflection would give us a good approximation for calculating the pressure at the chip-chip mount junction. The deflection of a cantilever beam under a load of *P* is defined as:

$$\delta = \frac{Pl^3}{3EI} \tag{4.5}$$

where, *P* is the load, *l* is the length of the beam, *E* is the modulus of elasticity for the beam material and *I* is the moment of inertia for the beam. The moment of inertia for the rectangular beam is calculated based on the width, *b* and height, *h* of the beam cross-section. So the equation for the cantilever beam deflection now becomes:

$$\delta = \frac{4Pl^3}{Ebh^3} \tag{4.6}$$

and the amount of load required to deflect the beam by a distance δ would be defined by:

$$P = \delta \frac{Ebh^3}{4l^3} \tag{4.7}$$

The following values correspond to the Be-Cu cantilever beam:

Young's Modulus, E = 124 GPa = 124,000 N/mm^2

Length of the beam, l = 3 mm

Width of the beam, w = 2 mm

Height of the beam, h = 0.05 mm

Deflection in the beam, δ = 0.1 mm

$$P = 0.1 \times \frac{124000 \times 2 \times 0.05^3}{4 \times 3^3} = 0.028703 \text{ N} \tag{4.8}$$

Total load on the Chip-Chip mount interface = 6 x P = 0.1722 N

Unfortunately, in case of the JJA chip, since the top of the silicon chip consists of a highly sophisticated circuitry, consisting of thousands of delicate junctions of niobiom-insulator-niobium connected in series, any kind of pressure applied to the top of the chip might result in the breakage of these junctions. Damage to even a single junction would result in a completely inoperable JJA chip. Keeping this in mind, any kind of contact with the top of the chip is completely avoided. As indicated by calculations, the amount of force exerted by the Be-Cu fingers is very less and does not contribute towards increasing thermal contact conductance between the JJA chip and the chip mount surface by causing deformation. Nearly all of the reviewed publications include much higher values of pressure as a dependent variable for their model; this makes it necessary for us to explore the options for a model independent of applied pressure.

4.4.2 Use of interstitial materials

The other efficient way of increasing the contact area is by the use of an interstitial material [63, 67-69]. As mentioned earlier, the use of interstitial material provides an alternate path for the heat flow between the surfaces. In the current model, the complete assembly of the JJA chip and the chip mount is kept under a vacuum of 1 mTorr; the presence of vacuum is necessary for reaching the cryogenic temperatures but also indicates that there would be not heat transfer by convection. By using an interstitial material between the two contacting surfaces, the vacuum present in the non-contacting region of the asperities is replaced by this material. For better performance the interstitial material selected should have high thermal conductivity at cryogenic temperatures. There were different options considered for the interstitial materials, the following discussion presents the experimentation with each.

4.4.2.1 Apiezon® N Grease

In many applications thermal grease is utilized for enhancing the heat flow at contacting surfaces. The biggest advantage that thermal grease offers is the ease of application and mostly they are very economical. The problem with the use of thermal grease, like silicone gel, is that because of low surface tension it has a tendency to migrate on other surfaces. The Apiezon® N grease is a high conductivity grease that provides an excellent thermal coupling medium between two interfacing surfaces [71]. Researchers have shown experimentally that the use of Apiezon® N grease has shown an increase of thermal conductance by up to a factor of 2 in certain cases [69]. Even though most of these experimental results consider the use of Apiezon® N grease along with the application of pressure, Apiezon N grease was used in our experiments. The Apiezon® N grease has characteristic that it is pliable at the room temperature but solidifies at cryogenic temperature. This characteristic at cryogenic temperature makes it ideal for mounting sensors and works well in holding samples at cryogenic temperatures. Unlike silicone based thermal greases, Apiezon® N grease claims to be migration resistant because of it being hydrocarbon based [71].

The pliability of Apiezon® N grease at room temperature allows an easy application in successfully filing the micro grooves on the chip mount surface. Initial tests indicated very promising results and there was a significant improvement observed in temperature attained at the chip location. The major shortcoming of using the thermal grease was observed after a few cycles of operation. The characteristic of Apiezon® N grease, of solidifying at the cryogenic temperature and remaining in the gel-form at room temperature, proved to be unfit in our design model. The design of the CCR based JVS

system is such that the complete assembly holding the JJA chip against the chip mount stays in a vertically upside down position. Once the system is turned off and stays at the room temperature, or at any temperature higher than the cryogenic temperature, the Apiezon N grease migrated out of the interface and on to the JJA chip. The presence of Apiezon N grease on the chip surface and the contact pads resulted in making the chip inoperable. The chip had to be sent back to the manufacturer for carrying out the complete clean up procedure. Even though the Apiezon® N grease has proven to significantly improve the thermal contact conductance during other experiments, in order to avoid damaging the chip again, it was not used at the interfacing junction of the JJA chip and the chip mount.

4.4.2.2 Indium Foil

Another very promising interstitial material considered was an Indium foil; Indium is a shiny, silver-white material that has the characteristic of being extremely ductile, malleable and is very soft. Also, it is corrosion resistant at room temperature and has a good ability to conduct electricity. Indium has a thermal conductivity higher than the Apiezon N grease [69, 72]. For the experimentation, a very high purity indium foil (99.99%), with a thickness of 0.005 inch (purchased from Lakeshore Cryogenics), was carefully cut to be of the same size as that of the JJA chip. The advantage of using an indium foil is that the foil always remains in the solid form and does not cause any contamination into the system. Once the indium foil is placed between the interfacing surfaces, application of a small amount of pressure causes the indium to ‘flow’ into the crevices and cavities, hence, filling the non-contacting regions caused due to the surface asperities.

Again, experiments were carried out using indium foil as the interstitial material. During these experiments the actual JJA chip was not used because of the possibility of damaging the chip. During the first stage of experiments a dummy silicon chip of the same physical dimensions as that of the JJA chip was used. The chip was mounted on the surface with indium foil as the interstitial material and a temperature sensor was attached to the top of this chip to monitor the temperature changes. Once it was observed that the chip temperature reached to at least 4.2 K, a non-functional JJA chip (provided by Dr. Clark Hamilton, NIST-Boulder) was used for the same experiment. The use of indium foil was proven very successful and the results obtained were very repeatable. With the use of an indium foil as the interstitial material between the OFHC copper chip mount and a 10 V JJA chip, several experiments were successfully conducted and the temperature achieved by the JJA chip, displayed by the I-V curves, were comparable to those achieved by the liquid helium based Josephson junction voltage standard system. Figure 4.6, represents the I-V curve obtained during one of these experimentations. In this I-V curve it can be seen that the leakage current due to temperature of the Josephson junctions is very low; further tests indicted that they were comparable to the results obtained with the same JJA chip used in a liquid helium based system.

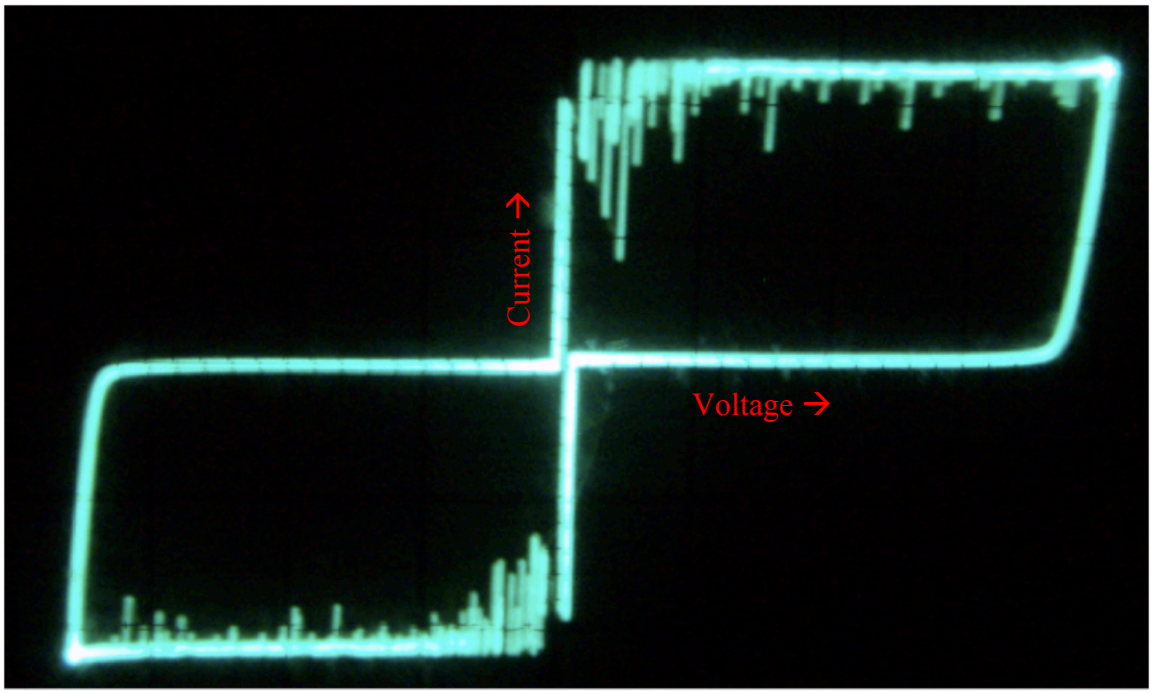


Figure 4.6: I-V curve obtained for the 10 V JJA chip.

The downside of using an Indium foil as the interstitial material is that it has to be pressed really well in order to establish a good contact with the surfaces. Applying a lot of pressure was not possible in case of the JJA chip, but a very good contact was established by pressing the indium foil well against the copper chip mount. The conforming of indium with the irregularities very efficiently solves the problem of thermal conduction by increasing the surface area of contact but poses another threat of creating localized stresses. The indium foil is pressed between the two interfacing materials at room temperature and under atmospheric pressure conditions. Once the system achieves a vacuum of 1 mTorr and reaches the cryogenic temperature, any air molecules trapped in the surface irregularities and under the indium foil forms high localized stress zones. Over the period of repeated warm up and cool down cycles these high stress zones may at any time damage the JJA chip. In our experience, in the course

of one of the experiments a 10 V JJA chip was cracked during the time of warm up cycle. Further communication with other researchers indicated that some other labs have also experienced issue of localized stress zones and breakage while using an Indium foil[73, 74].

The microwave power incident on the JJA chip has the capability of heating the chip above a temperature of 8 K. The bias supply generates only about 0.2 mW maximum heating, where as, the microwave dissipation for optimum step generation in near 15 mW. VMetrix and Hypres have reported that during the use of microwave power, heating of the chip to a higher than operable temperature occurs because of inadequate cooling with Indium foil under the chip [73, 74]. Also, since by itself Indium displays superconducting behavior at a temperature of 3.4 K, it is considered too close to be operating in the temperature range of 3.9-3.6 K. At that temperature, Indium has a tendency of forming superconducting junctions with other metals and hence should be avoided operating at temperatures lower than 5 K. After these series of experiences, research was initiated in developing a mounting technique that would achieve the required operational temperature without the use of any interstitial material.

4.4.3 Mounting- Diamond Turned Machining

In the previous sections we looked into the different techniques that have been investigated for mounting the JJA chip and creating an interface with the OFHC copper chip mount surface. Even though each technique had its own advantages and some of them were successful in attaining the required operating temperature at the chip surface, the investigated methods were not perfectly suitable for the JVS system because of their drawbacks. In the CCR based JVS system, because of purely conductive cooling of the JJA chip a good surface contact between the bottom of the JJA chip and the top of the

chip mount assures efficient and fast cooling of the chip. As discussed in section 4.3, the interfacing surfaces of the JJA chip and the conventionally machined chip mount seemed to have good physical contact on the macroscopic level, but instead revealed the presence of surface roughness that led to the surfaces contacting only at discrete points. Apparently, the actual area of contact is only a fraction of the cross sectional area considered earlier. We therefore decided to explore other methods for increasing the contact area and obtaining a better conduction path; the approach considered was to physically alter the surface asperities on the chip mount surface by means of mechanical polishing, lapping and/or machining.

The process of lapping and polishing precisely removes material from the workpiece and can be used to obtain the specific surface roughness. While lapping the chip mount surface it was necessary to take into consideration the very little amount of material that could be safely taken off without affecting the electrical contacts. As discussed during the design of the JJA chip mount, in section 3.4, the FR-4 circuit board has Be-Cu fingers that connect to the bond pads on the JJA chip establishing electrical contact with the JVS system controller. Lapping the chip mount surface would lower the height of the JJA chip and increase the distance from the FR-4 circuit board. The consequence of increasing the distance is twofold; one, it reduces the pressure on the JJA chip surface, thus reducing the thermal contact conductance (since it is dependent upon the pressure at the interfacing surfaces) and two, the electrical connection with the JJA chip bondpads might be lost.

Lapping the copper surface gives a very smooth surface but there are instances where microscopic particles get ingrained in the surface, which tend to create random high spots. These unwanted high spots on the interfacing surface creates pressure points in the

chip and during the thermal cycling has a tendency of damaging the JJA chip. Another problem encountered with the polishing procedure was the rounding of edges. The JJA chip rests on a pedestal on the chip mount that has the same dimensions as that of the chip. The flatness of the pedestal is a very important and crucial parameter for a good thermal contact conductance as well as for the safety of the JJA chip. Because of the above mentioned issues, the lapping and polishing operations must be executed carefully. Note that the original chip mounts did not have a surround, but instead just the pedestal on which the chip rested [20]. In one instance, lapping the pedestal resulted in rounding of the edges and the chip was therefore overstressed to failure. Subsequent mounts were fabricated by machining a "mote" around the pedestal, with a surround outside the "mote" that would ensure the chip mount was held flat against the lapping surface and prevented rounding of the pedestal surface.

The Center for Precision Metrology at the University of North Carolina at Charlotte offers cutting edge technolgy in the field of high precision machining facilities. A single point diamond turning is a state-of-the-art machining technique capable of achieving roughness in the nanometer range and mirror like reflective surfaces. In diamond turning the work material is continiously rotated with respect to the tool and the cutting tool is positioned normal to the face of the work surface. In the single point diamond turning process, diamond is used as the cutting edge material for the tool. Since diamond is the hardest material available, the cutting edge of a single crystal diamond tool has far greater edge smoothness and edge sharpness than other cutting tool materials. Figure 4.7 gives a diagrammatic representation of the single point diamond turning operation and shows the picture taken during the machining operation at UNC-Charlotte.

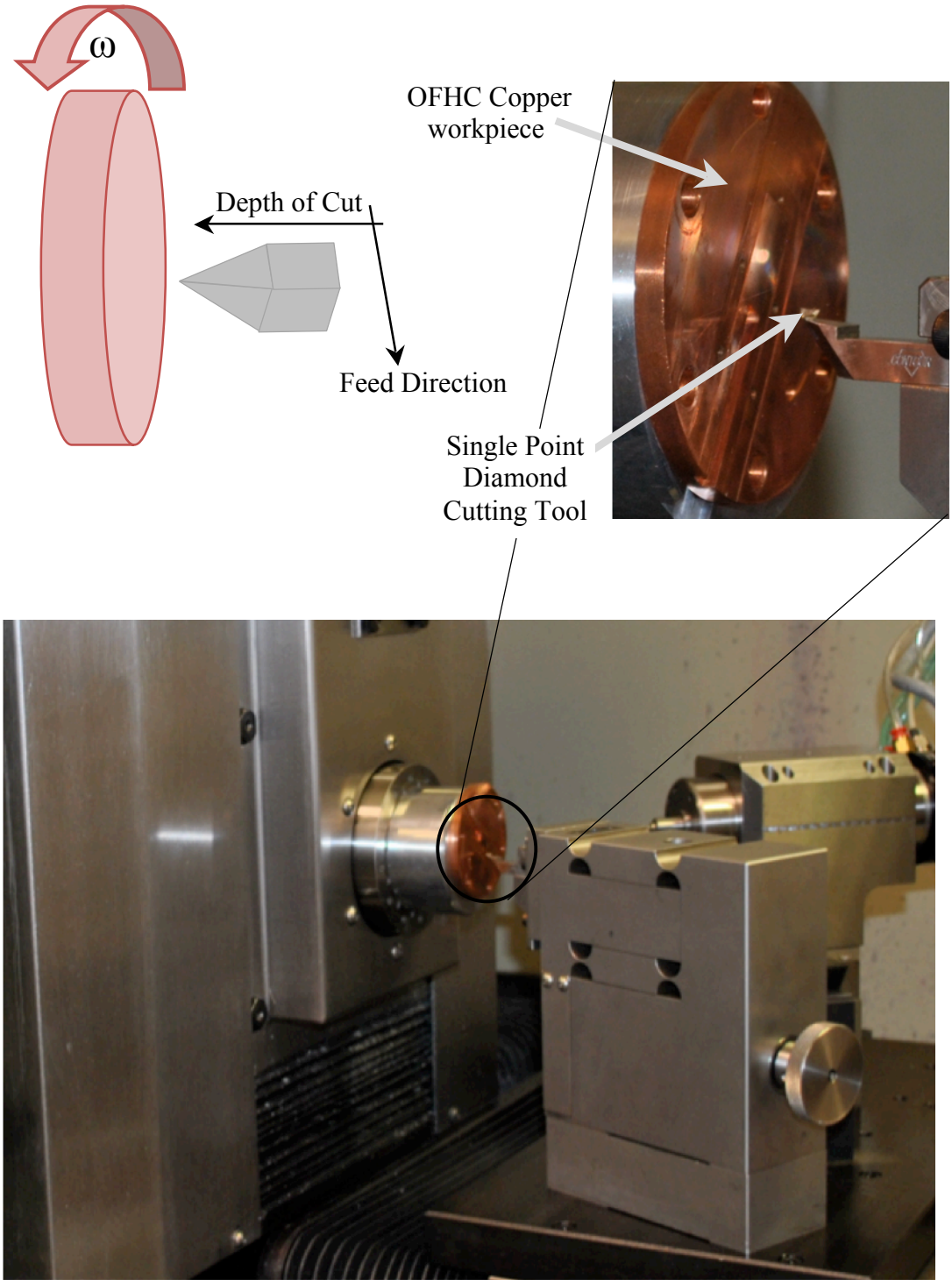


Figure 4.7: Schematic representation and picture of actual diamond turning operation.

The diamond turning was done on a Moore Nanotechnolgy systems Nanotech 350FG and the final surface finish can be varied by changing the depth of cut and feed for the machining tool. Figure 4.8 shows the image of the copper chip mount after diamond turning; the highly reflective mirror-like surface finish can be seen and the insert shows a microscopic image comparison between the diamond turned surface at the raised pedestal and the previous conventionally machined surface.

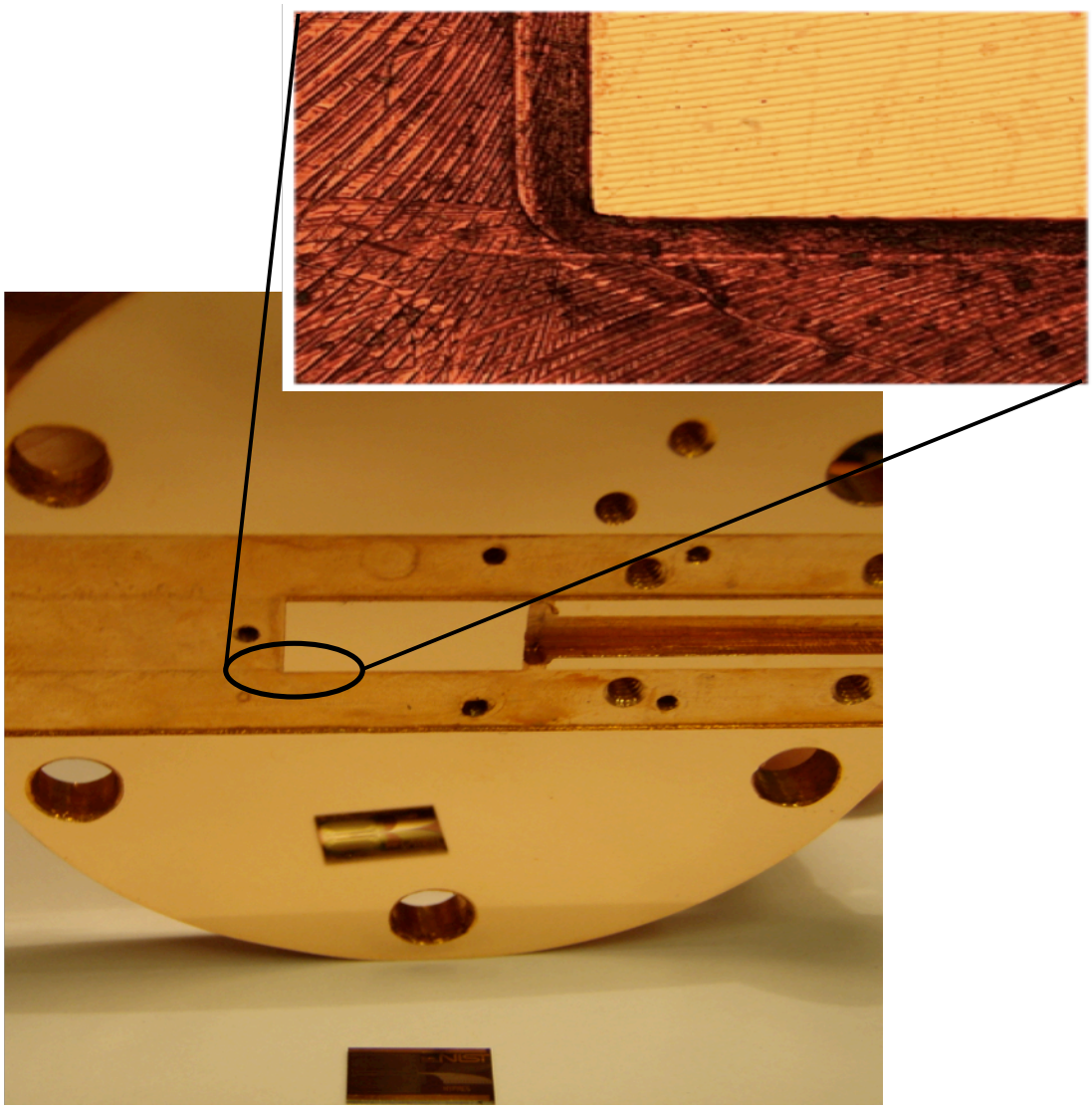
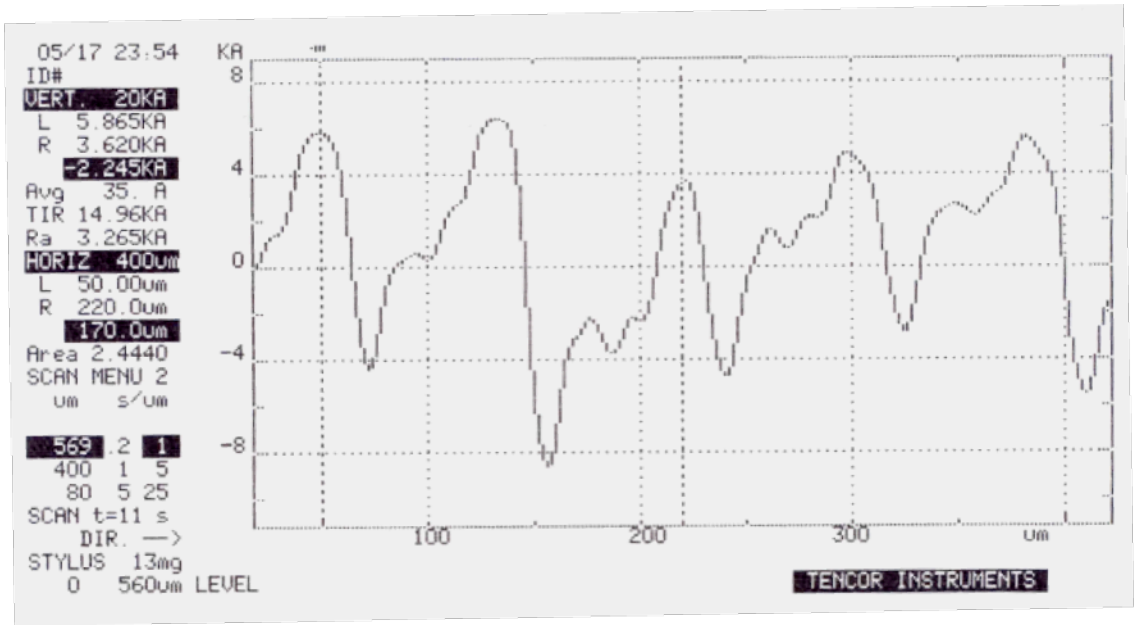
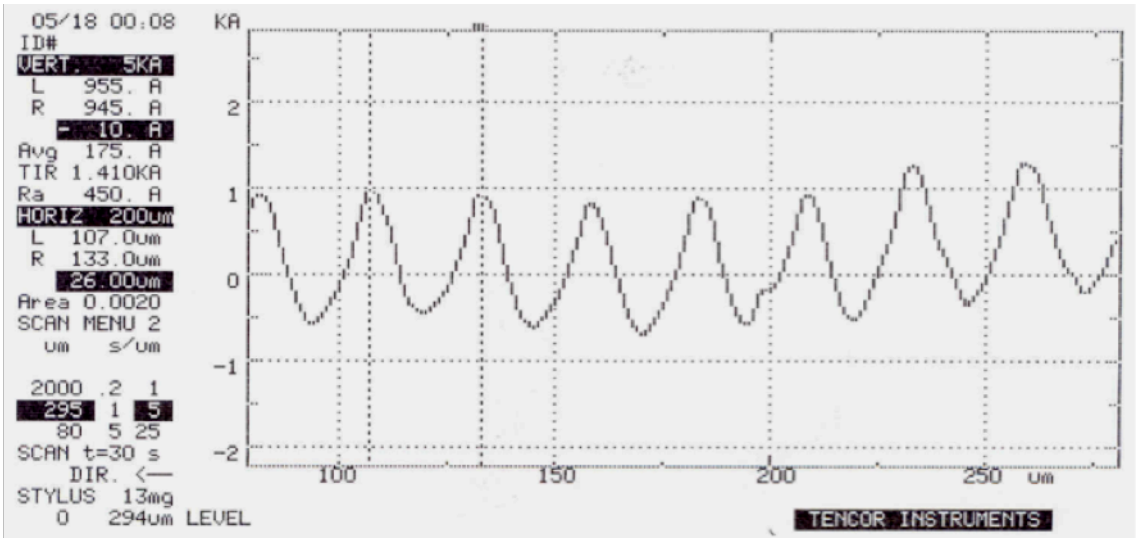


Figure 4.8: Picture of the diamond turned copper chip mount surface and the microscopic image for surface roughness comparison.

Figure 4.8 shows a clear representation of how significantly the surface profile for the copper chip mount changed after the diamond turning operation was performed. The shiny and reflective surface is a clear representation of surface roughness, which was found to be in the nanometers. Section 4.3 discussed how the measurements taken on the Alpha step profilometer provided an accurate representation of the surface profile; the profile seen in Figure 4.4 was an indication of the rough surface and also the significantly varying locations for the various peaks and valleys on the surface. After diamond turning the surface of the chip mount, the surface profile measurements were again taken and are compared in Figure 4.9 and it can be seen how the roughness profile of the chip mount surface has significantly changed. Looking at the profile measurements of the two surfaces the most significant difference is in the peak-to-valley amplitude. In the previous case, as can be seen in Figure 4.9 (a), the peak-to-valley height is in the range of 0.8 μm to 1.4 μm and the peak-to-peak distance is approximately 85 μm. For the diamond turned surface these numbers are significantly different with a peak-to-valley distance of nearly 0.15 μm and the peak-to-peak value of approximately 26 μm. By decreasing the peak-to-peak distance for the contacting surface, the number of actual contacting points has increased threefold. Also, it is evident how the variation in the distance of the peaks from the hypothetical contacting plane is significantly lower, thus providing with more contact points for the interface. As we know from the equation for the heat flow, $Q = h_c.A\Delta T$, the rate of heat flow across the contacting interface is proportional to the cross sectional area of contact. So by increasing the number of contacting points and hence the contacting area the heat flow across the JJA chip and chip mount interface was significantly increased.



(a): Alpha step profilometer plot for the conventionally machined chip mount surface



(b): Alpha step profilometer plot for the diamond turned chip mount surface

Figure 4.9: Surface profile measurement and comparison of conventionally machined surface and diamond turned surface.

A comparison of the plots from Alpha step profilometer for the conventional machined surface before and after the diamond turning operation is carried out and presents a clear indication of the change in surface profile. Based on the measurements from Figure 4.9, the frequency of waviness for the diamond turned surface is nearly 3.27 times higher than that for the conventional machined surface (wavelength, λ = 26 μm and 85 μm, respectively) and the amplitude of waviness is about 10 times lesser (Peak-Peak = 0.15 μm and 1 μm, respectively).

The profilometer plot seen in Figure 4.9 is a very good representation of the overall surface profile for the conventional machined chip mount surface as well as the diamond turned surface. As shown in the figure, the peaks on the chip mount surface do not lie in the same horizontal plane and the height of these peaks vary significantly. In order to analyze the effect surface roughness may have on thermal conductivity, a simple analysis was conducted where the peaks of the machined surface would deform under pressure of the JJA chip surface, here assumed to be perfectly flat. Although the actual amount of deformation is unknown, one can see that under moderate loading fewer peaks of the conventionally machined mount would actually contact the chip as opposed to the case of the diamond turned surface.

One of the ways in which the high points can be brought closer to the plane is by applying some pressure on the chip that would either elastically or plastically deform the surface. The amount of pressure that can be applied is limited by the properties of the materials used. Looking at the surface profiles in Figure 4.9, it can be seen that in order to bring the ‘high-points’ to an intersecting horizontal plane a deformation of about

0.025µm would be required on the diamond turned surface as compared to a deflection of about 0.2 µm in case of the conventional machined surface.

To get a better understanding of the change in surface profile before and after the single point diamond turning operation is carried on the surface, a graphical representation of the two surfaces is presented in Figure 4.10.

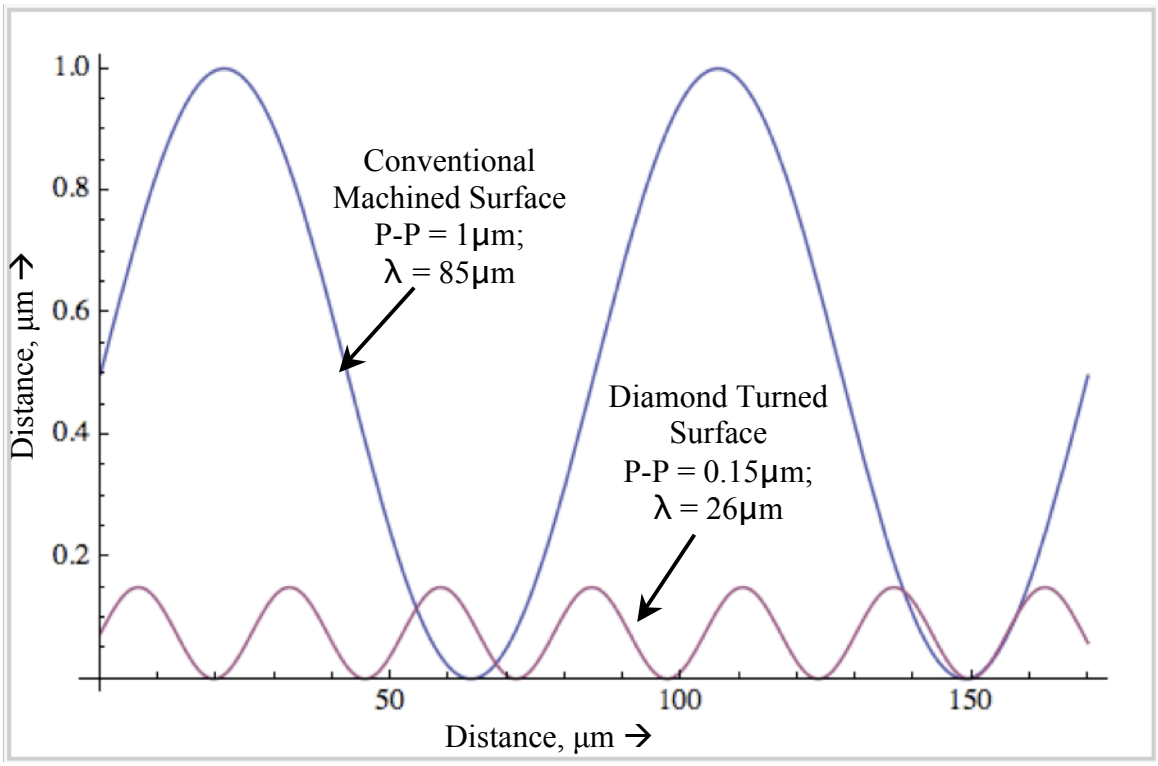


Figure 4.10: Graphical representation of the conventional machined and diamond turned surface.

The representation of surface profile in Figure 4.10 is the best case scenario comparison for the two surfaces. To derive a mathematical model for the approximate representation of the surface profile, let us consider that the surface is absolutely flat and all the high points are on the same horizontal plane. Modeling the loaded chip as deforming the three highest peaks of Figure 4.9 (noting that more or less would come into

play depending on preload), a simple assumption would be that only three of the conventionally machined peaks, over the given range, contacted the chip as opposed to 10 of the diamond turned surface. The next step in modeling the contact area (and therefore thermal conductivity) is to graphically represent the peaks of the respective machined surfaces as cylinders with hemispherical tops, as shown in Figure 4.11. If we consider the JJA chip surface to be flat and in contact with the chip mount surface, we can estimate the contact area between the two surfaces based on the foot print of the JJA chip. The peaks of the contacting surface on the chip mount can be approximated by a curve fit representation where the complete surface profile can be replaced by a cross-section as seen in Figure 4.11. The radius of the circular tip is approximated by fitting a curve for the sine wave representation of the surface profile. This allows us to assume a cylindrical Hertzian contact interface at each asperity [75].

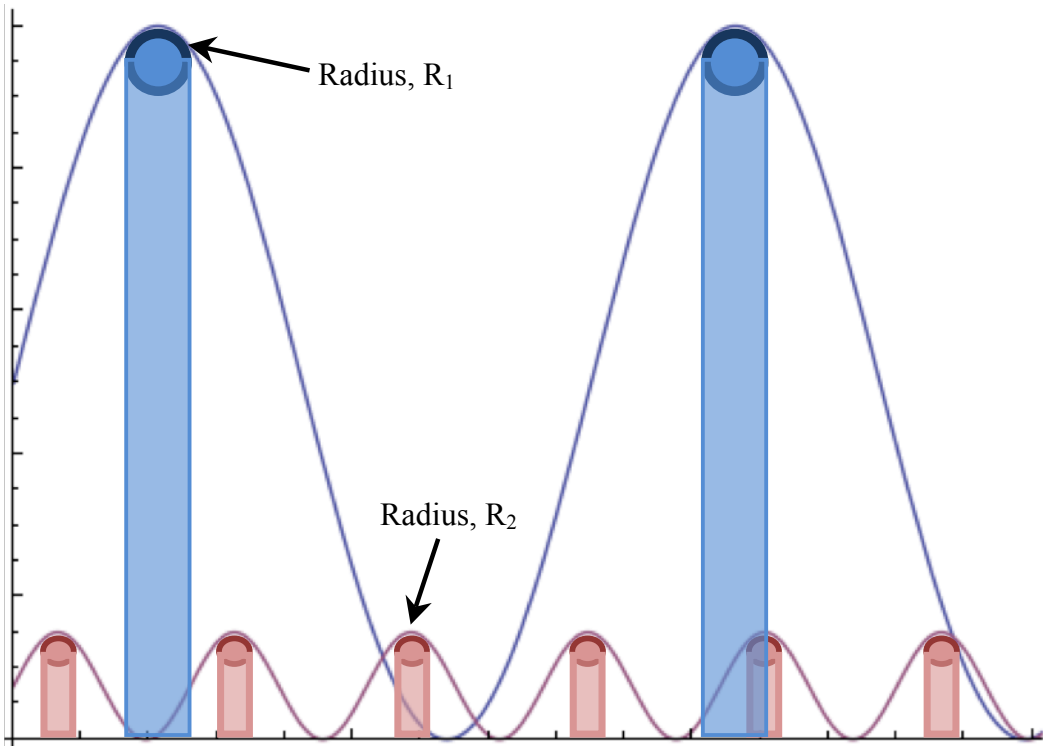


Figure 4.11: Curve fit representation for approximating the contacting tip radius.

Further, looking at the surface profile in the 3rd dimension, a line contact is assumed along the length of each surface peak. Figure 4.12 shows that the complete model can be approximated as a series of cylinders separated by the distance λ and having a length equal to the width of the JJA chip. If there is a pressure applied at the interfacing junction it might result in deforming the asperities and hence increasing the contact area between the two surfaces. If we assume a constant pressure, *P* at the contacting surface and follow the mathematical theory developed by Heinrich Hertz [75], it may be possible to estimate the deformations produced by the pressure of a plate on the cylinder. According to the theory, if we assume a Hertzian contact between the two surfaces, an incident load, *P* causes an increase in the rectangular contact area with a width of *b*.

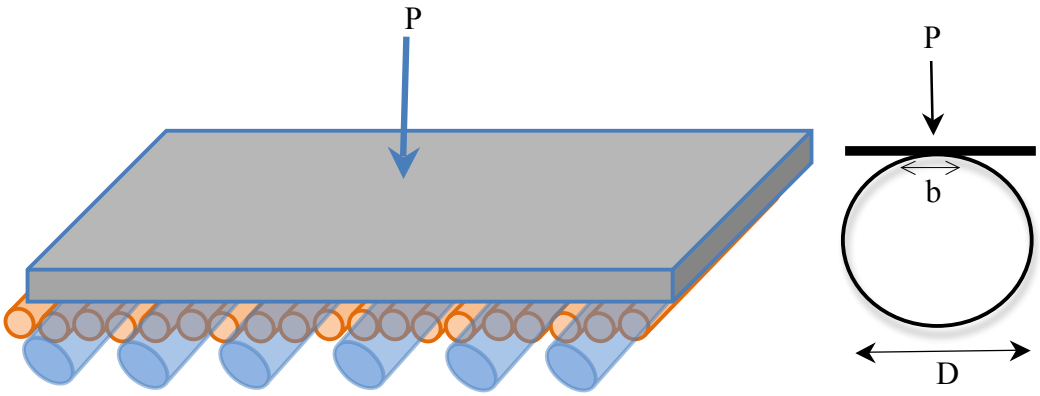


Figure 4.12: Hertzian contact representation for cylinder and flat plate. The small and large cylinders represent diamond turned surface and the conventionally machined surface, respectively.

The width of the rectangular contact area, b is given by [75]

$$b = 1.60\sqrt{pK_D C_E} \tag{4.9}$$

where, p is the load per unit length for a load P; K_D = D, for the case of a cylinder on a flat plate and $C_E = \frac{1-\nu_1^2}{E_1} + \frac{1-\nu_2^2}{E_2}$, with ν = Poisson's ratio and E = modulus of elasticity for the two intersecting bodies 1 and 2.

The two cases considered are that for the conventional machined surface and for the diamond turned surface. If λ_1 and λ_2 are the wavelengths for the conventional machined surface and the diamond turned surface, respectively, and L and W the length and width of the JJA chip, the load per unit length, p is

$$p = \frac{P}{l} \tag{4.10a}$$

where, total length of contact, l is

$$l = L\frac{W}{\lambda} \tag{4.10b}$$

So, for the case of conventional machined surface,

$$b_1 = 1.60\sqrt{P\frac{\lambda_1}{WL}D_1C_E} \tag{4.11}$$

and for the diamond turned surface,

$$b_2 = 1.60\sqrt{P\frac{\lambda_2}{WL}D_2C_E} \tag{4.12}$$

The rectangular area of contact for the applied load P can thus be given as the product of the contact area width, b and the total length of contact for the chip surface. The area of contact for each case is,

$$\mathrm{A}_1 = b_1\, l_1 \tag{4.13}$$

where l_1 is the total length of contact between the two surfaces. Combining equations (4.13) and (4.11)

$$A_1 = 1.60 l_1\sqrt{P\frac{\lambda_1}{WL}D_1C_E} \tag{4.14}$$

$$\text{or,}\quad A_1 = 1.60\sqrt{P\frac{WL}{\lambda_1}D_1C_E} \tag{4.15}$$

and in the same way,

$$A_2 = 1.60\sqrt{P\frac{WL}{\lambda_2}D_2C_E} \tag{4.16}$$

So, the ratio of change in area for the case of conventional machined surface and the diamond turned surface is given by,

$$\frac{A_2}{A_1} = \sqrt{\frac{D_2}{D_1}}\sqrt{\frac{\lambda_1}{\lambda_2}} \tag{4.17}$$

Now, from our measurement of the surface profile done with the alpha step profilometer we know the values for λ_1 = 85 μm and λ_2 = 26 μm, also, if the values for D_1 and D_2 are estimated to be around 10 μm and 5 μm, respectively, the ratio of change in area can be calculated to be approximately,

$$\frac{A_2}{A_1} = 1.3 \tag{4.18}$$

This analysis assumes uniform peaks, as seen in Figure 4.11, but Figure 4.9 (a) and (b) clearly shows the likelihood that lesser number of peaks in the case of conventional machined surface come in contact with the JJA chip as compared to the diamond turned surface. Hence, the change in area by a factor of 1.3 is a conservative approach and it can reach 1.5 -1.8. Assuming the incoming heat into the chip from the microwave source is q = 0.1 W, one can assume that the chip is hotter that the cold head, which is approximately 3.6 K under no load (measured). Since, $q = kAdT$, it follows that the heat flowing from the chip to the chip mount increases by 30% and causes a 30% difference in temperature.

A 1.3 fold change in the contacting surface area is a significant increase gained by diamond turning the chip mount surface; this change in surface area translates directly to a better temperature achieved at the JJA chip. Earlier, operating at the temperature of 6 K,

this change in the surface area caused a change in temperature close to 1.5 K and a final temperature of 4.2±0.2 K was experimentally achieved. By diamond turning the chip mount surface, not only was the waviness of the surface reduced, but also the surface roughness was significantly reduced to less than 4 nm. The surface profile measurement

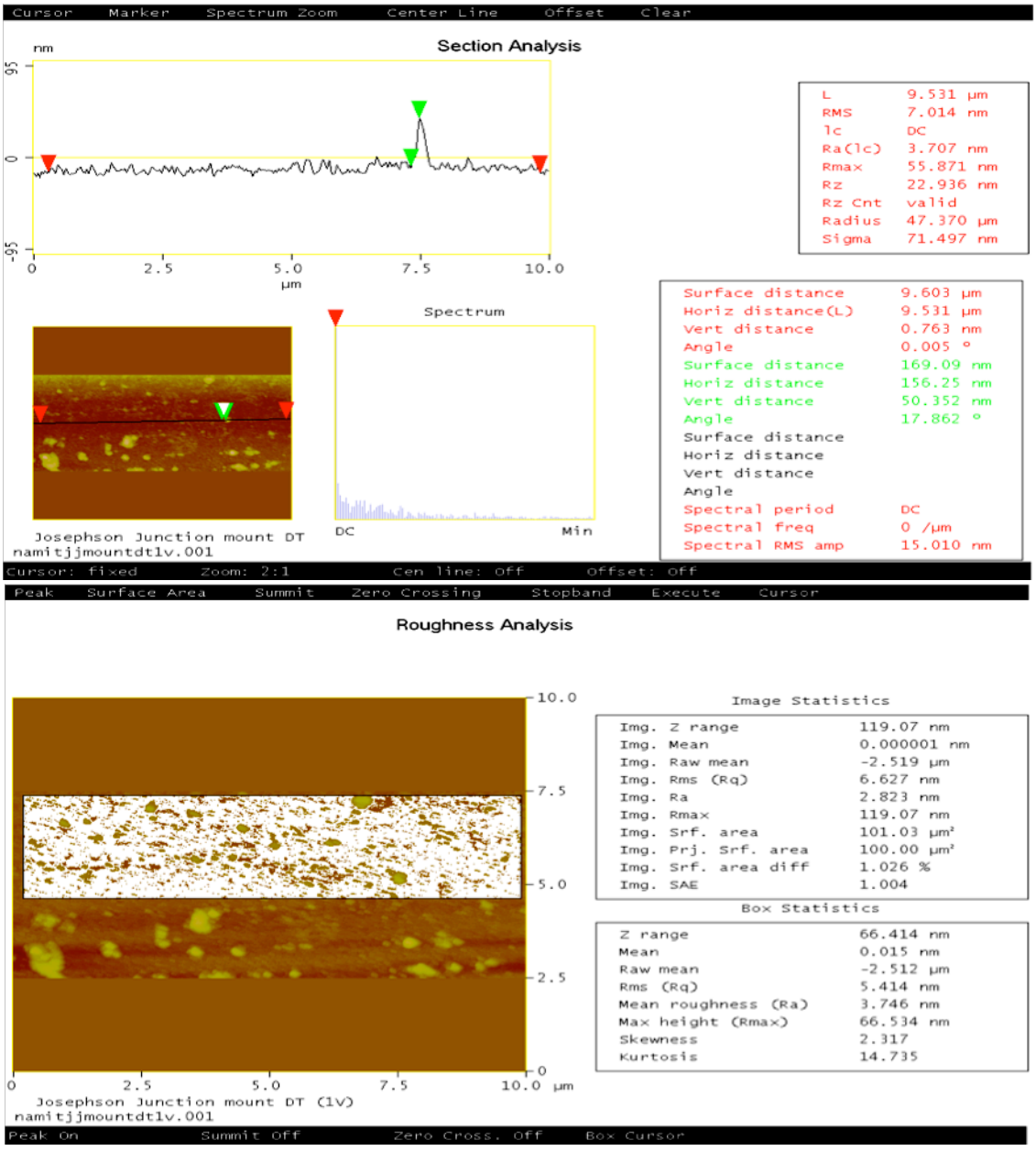


Figure 4.13: Atomic Force Microscope (AFM) measurements for the diamond turned surface.

and the roughness analysis done on an Atomic Force Microscope (AFM) is shown in Figure 4.13.

Experimentally, the change in thermal contact conductance at the interface of the JJA chip and the OFHC copper chip mount was verified upon cooldown of the chip. Previously, it was observed that even though the chip mount was reaching a temperature of lower than 4 K, the JJA chip resting on the chip mount surface was unable to achieve the same temperature. After investigation it was concluded that the unexpectedly low thermal contact conductance at the interface of the JJA chip and the chip mount was causing the chip to not cool sufficiently. After experimenting with different mounting techniques for the JJA chip, the diamond turning of the chip mount surface was considered as a more permanent solution for the thermal conductance problem. The diamond turned surface had very low roughness values and demonstrated very promising surface characteristics, based on the different measurements shown earlier.

The ultimate test for the diamond turned surface was to successfully cool the JJA chip to the required operating temperature of 4.2 K. There were two independent methods adopted to determine the temperature at the Josephson chip. First, a dummy silicon chip was precisely cut to the dimensions of the JJA chip and was placed at the location of the JJA chip. A silicon diode temperature sensor was mounted on top of a dummy silicon chip and the system was operated through the regular operating thermal cycle. During this experiment, for comparison purposes, another temperature sensor was monitoring the temperature at the chip mount surface. After pulling the required vacuum and operating the cryocooler for 180 minutes, a temperature of 3.6 K was observed at the chip mount surface and a temperature of 4 K was measured on the silicon chip. After repeated

experimentations it was confirmed that the diamond turned surface interface provided the thermal contact conductance required for cooling the JJA chip.

The second method of determining the temperature of the JJA chip was to observe the Current-Voltage (I-V) characteristic and the critical current for the JJA chip. The I-V curve for the 1-volt JJA chip was observed and as a reference it was compared with the I-V curves provided by the manufacturer (Hypres Inc.) of the JJA chip. The I-V curves obtained by Hypres were the best-case scenario and were measured by cooling the JJA chip in liquid helium Dewar. By observing the I-V curves for the JJA chip it was confirmed that the chip was getting sufficiently cooled in order to operate as the voltage standard. Further, the comparison of the results with those attained by Hypres using the liquid helium cooling system proves that the CCR based system designed and assembled at UNC Charlotte successfully operated at the required temperature of 4.2 K. Further discussion of results is conducted in Chapter 6.

CHAPTER 5: MAGNETIC FIELD CHARACTERIZATION

The design of an efficient Josephson junction voltage standard system is critically dependent on insulation from sources of magnetic noise. One of the most common difficulties in achieving proper operation of the JVS system is a phenomenon called "magnetic flux trapping". During the cool down of the JJA chip, as the superconducting junctions transition from the normal conducting state to superconducting state, presence of any magnetic field is trapped in junctions and offers resistance to the flow of superconducting current. In operating the typical helium Dewar based JVS system, the JJA chip attached to the cryoprobe is very slowly lowered into the liquid helium bath; lowering at a faster rate causes sudden quenching and there is an increased chance of magnetic flux getting trapped in the Josephson junctions. If magnetic flux is trapped in any junction, the cryoprobe is pulled out of the bath and is kept at that position till the chip reaches a temperature higher than the critical temperature of niobium. This operation is painstaking and sometimes is repeated several times before the acceptable I-V characteristics are obtained. In the CCR based system, the cooling of JJA chip is gradual and the use of magnetic shields allows the chip to be placed in a very low magnetic field chamber, hence, greatly reducing the chance of flux trapping. In case there is flux trapping observed in the JJA chip, the cryocooler is turned off and after reaching a temperature higher than the critical temperature the cooling cycle is started again.

5.1 Magnetic Field and Superconductors

In Josephson junctions, the Cooper pair of electrons has a small binding energy and is very sensitive to any external source of excitation. Presence of external magnetic field exerts torque on the electron spins, which tend to break up these Cooper pairs and as the Cooper pairs separate into individual electrons the material becomes a normal conductor or ‘non-superconductor’. The breaking of Cooper pairs occur in the presence of magnetic fields higher than a particular value associated with the superconductor material; this magnetic field value is referred to as the critical magnetic field and is dependent on the material involved.

When two superconductors are separated by a thin insulating layer to form a Josephson junction, the quantum mechanical tunneling of Cooper pairs occurs without breaking up the pairs. The Cooper pairs on each side of the junction can be described with an exponential wavefunction similar to the free particle wavefunction. In the absence of electric current, Cooper pairs in the superconductor can be described by a single wavefunction because all the pairs have the same phase i.e. they are "phase coherent". In this condition, wavefunctions for Cooper pairs on each side of the junction penetrating into the insulating region are “phase- locked”.

The Cooper pair has always been thought of as having behavioral characteristics of an elementary particle when characterized by size, electric charge, spin, mirror-reflection and time reversal properties. But some of the recent research presents a contrary theory proposing that superconducting electron pairs are not unchanged elementary particles, but rather complex objects with characteristics that depend on the strength of the magnetic field that they are exposed to [76]. According to Andrei Lebed, powerful magnetic fields

appear to change the physical nature of superconductivity with some quite unusual effects, but this theory still awaits experimental proof [76].

5.2 Critical Magnetic Field

The superconducting state cannot exist in the presence of a magnetic field greater than the critical magnetic field, even at absolute zero. This critical magnetic field is strongly correlated with the critical temperature for the superconductor, which is in turn correlated with the bandgap. The critical temperature and the critical field are the parameters that represent the energy that can be supplied to the material in a way that it starts to interfere with the superconducting mechanism. According to the Meissner effect, the nature of superconductors is to exclude magnetic fields but this is true only as long as the applied field does not exceed its critical magnetic field. The critical magnetic field value is typically established at 0 K, decreasing in magnitude with increasing temperature until it reachs zero at the critical temperature for superconductivity. The critical magnetic field (B_c) at any temperature (T) below the critical temperature is given by the relationship [77]

$$B_c = B_c(0)\left[1-\left(\frac{T}{T_c}\right)^2\right] \tag{5.1}$$

where, $B_c(0)$ is the field required to quench superconductivity at 0 K and T_c is the critical temperature for the material. For niobium, the value of $B_c(0)$ is 2060 Gauss and T_c is 9.2 K [77]. Hence, for a Niobium device operating in the vicinity of 4.2 K, the critical magnetic field value is 1630 G. It is essential to design the system in such a way that the magnetic field at the JJA chip should be well below 1630 G in order for niobium to retain its superconductive behavior. For operating a Josephson junction device made of

niobium, a magnetic field of 1630 G is still too high to attain a stable operating condition as these junctions are highly sensitive to any exposure of magnetic field and can easily be affected by the presence of fields as low as a few Gauss.

5.3 Magnetic Shielding

The presence of magnetic field in a region is the result of a source of magnetic flux, which might be the Earth, a motor, transformer, electric power line, etc. The strength of magnetic field at a location is dependent upon the source and the separation from the source. In case of the JVS system, proper electro-magnetic shielding is critical to isolate the JJA chip from these electro-magnetic fields. The best practice to isolate devices from a known source of electro-magnetic field is by removing the device from the field; however, that is often not possible. In this case, increasing separation from the source will lower the strength of the field to be shielded. Finally, there are a number of shielding materials that can serve to further reduce the incoming electromagnetic fields.

In order to develop and design an effective magnetic shield, it is essential to first measure the intensity of magnetic field surrounding the area to be shielded and have an estimate of the sources of electro-magnetic noise. In the Josephson voltage standard (JVS) system, it is crucial to electro-magnetically shield the Josephson junction array (JJA) chip and maintain a very low level of magnetic noise in the vicinity. In the UNC-Charlotte JVS system, a closed-cycle refrigeration (CCR) based cooling system uses a two-stage 4.2 K Gifford-McMahon (GM) cryocooler and vacuum pump to achieve the operational temperature; the disadvantage of using these systems is that they are major sources of electro-mechanical noise and are in the close vicinity of the JJA chip. Since the source of noise cannot be eliminated, nor the separation distance significantly

increased, magnetic shields must be carefully engineered around the chip to obtain a very low magnetic field region.

Magnetic shields are created using ferromagnetic materials with very high magnetic permeability. Since the magnetic fields can neither be created nor destroyed, the purpose of magnetic shielding is to re-arrange the magnetic fields in such a way that a region of zero or very low magnetic field is created surrounding the device to be shielded. The high-permeability ferromagnetic material shields the region by pulling the magnetic field towards itself and away from the device to be shielded. The alloy compositions of many magnetic shield materials are proprietary to the manufacturers, and a material known as MuMetal® is regarded as the most suitable for creating the magnetic shield for the JJA chip. The MuMetal® shield has the ability to absorb magnetic energy and results in very high attenuation by concentrating the magnetic field within the MuMetal® shield itself, making these shielding alloys the materials of choice for reducing low-frequency electromagnetic interference (EMI).

An enclosure of very low magnetic field region was created for the JJA chip by fabricating two concentrically spaced magnetic shields from high permeability MuMetal®. Since, the sources of magnetic fields are very strong and close to the JJA chip, the multiplying effect of successive shields provides substantially greater attenuation of magnetic fields and prevents saturation of the shield as compared to a single magnetic shield of equivalent wall thickness. Each magnetic shield consists of a cylinder with one closed end and a close-fitting removable cover on the other end. Each shield is magnetically isolated from the adjacent shield by nonmagnetic OFHC copper spacers. The inside chamber diameter is kept as small as possible because attenuation is

inversely proportional to diameter. The size of the magnetic shields is calculated based on the approximation of the ambient field and the desired level of flux density inside the chamber. This calculation is done based on equation 5.2 [78]:

$$B = 1.25\frac{D.H_o}{t} \tag{5.2}$$

where, B is the flux density in the shielded region, D is the diameter of the shield, H_0 is the ambient field in Oersteds and t is the thickness of the shield.

A hole is provided in the side wall of each layer of magnetic shield for the RF-waveguide and signal cables. Unfortunately, a hole in the magnetic shield allows the interfering field to fringe into the chamber; the amount of leakage is a function of the hole size and the angle between the axis of the hole and the direction of the interference field. In order to reduce leakage through these access holes, they were kept as small as possible with their axes positioned perpendicular (transverse) to the ambient field.

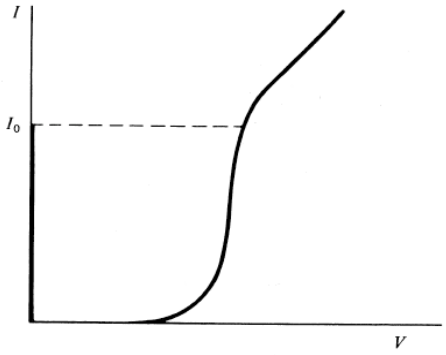
The attenuation of magnetic field achieved by using a magnetic shield is specified by a term known as the attenuation factor. The attenuation factor is a ratio of measured field before shielding to that measured after shielding. A single layer of MuMetal® shield provides 30 to 40 db attenuation, and higher levels can be achieved by using multiple layers. The attenuation ratio is given by the equation 5.3, where t is the thickness of the shield, μ is the permeability and D is the diameter of the shield [78].

$$\text{Attenuation ratio, } A = \frac{\mu.t}{D} \tag{5.3}$$

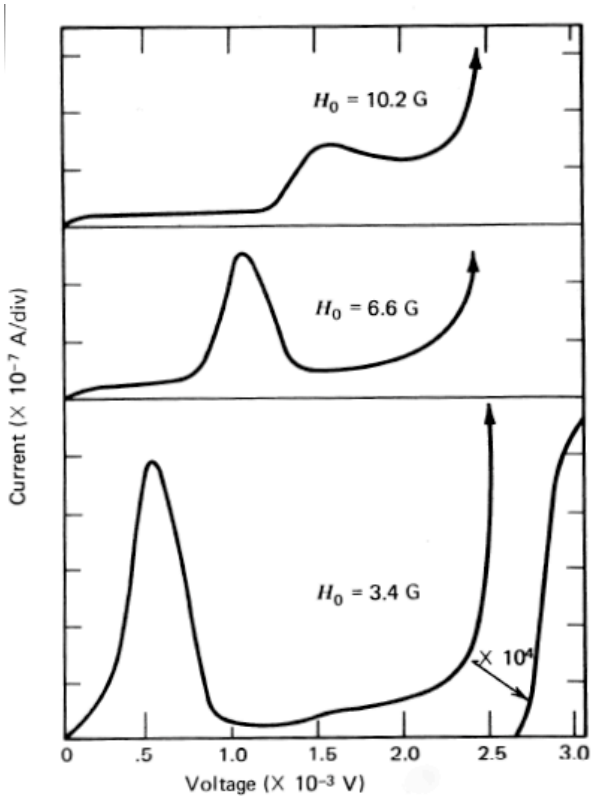
MuMetal® has maximum magnetic shielding properties and minimal outgassing, making it the appropriate choice for high vacuum and low temperature applications. However, at cryogenic temperatures the permeability of MuMetal® decreases as the

temperature drops because of reduced molecular mobility and the attenuation is reduced.

The Josephson junctions made of superconductive material are highly sensitive to the presence of magnetic fields. Even though the modern junctions, fabricated with thin-film technologies, are a little more forgiving to the presence of magnetic fields in the direction perpendicular to the junction plane, the performance of these junctions deteriorates rapidly with the presence of fields. Figure 5.1 (a) shows the I-V characteristic curve when a dc voltage is applied to a Josephson junction. A dc Josephson current appears at $V = 0$, signified by the straight line along the y-axis. As the current through the superconducting junction exceeds the critical current value I_0, the superconducting property is destroyed and we obtain the normal conducting state. Because of the presence of magnetic field, the junction is unable to achieve the critical current value at $V = 0$ and the superconducting state is never reached. Figure 5.1 (b) shows the dependence of critical current in the Josephson junction to the presence of magnetic field perpendicular to the junction surface and the I-V relationship in the presence of 3 different magnetic fields, namely, 3.4 G, 6.6 G and 10.2 G is plotted. In this case, the linear superconducting current, represented by the straight line on the y-axis in Figure 5.1 (a), is shifted to a non-zero voltage and takes on the shape of a bell-curve. As the external field increases, this characteristic curve is shifted to the right and further away from the superconducting behavior. Figure 5.1 shows how the presence of even a few Gauss can completely make the junction dysfunctional. The magnetic shield was therefore designed to always maintain a field closer to 1 Gauss at the JJA chip location.



(a) I-V characteristic of a Josephson junction in absence of magnetic field [77].



(b) Loss of superconducting state due to presence of magnetic field [27].

Figure 5.1: Dependence of Critical Current on incident magnetic field.

It is known that the presence of magnetic field in the vicinity of a JJA chip affects the operation of the JVS system, but there was no literature found that quantifies the presence of magnetic field strength to the performance of a JJA chip. Several experiments were

conducted to study the occurrence of flux trapping during the cool down cycle with respect to the amplitude of magnetic field present at the JJA chip. Since there was no conclusive evidence of what the critical value for fields was, we chose to minimize as much as possible and then conducted experiments to see what values resulted in superconductivity. The chance of flux trapping increases with a field higher than 5 Gauss and operating at fields closer to 1 Gauss drastically reduces the chance of trapping. Based on these experiments, the MuMetal® magnetic shields were designed to achieve an enclosure with field strengths of 1 Gauss or less.

The JJA chip sits on a 2.75" diameter, round mounting surface machined from OFHC copper. The chip is positioned at the approximate center of the plate. The MuMetal® magnetic shields are designed in such a way that they completely enclose the JJA chip along with the mounting surface. The first layer of cylindrical magnetic shield has a diameter of 2.9" with a height of 0.75" and the second shield has a diameter of 3.35" with a height of 2.5". The thickness of shield material used was selected to be 0.02". As discussed earlier, the magnetic shield provides the shielding effect by attracting the magnetic fields towards it and providing an alternate path for the fields. Because of this, the surface of the magnetic shields has a much higher concentration of magnetic field and hence it is very important to separate the two layers of shield with a non-magnetic material. A separation of 0.35" is achieved between the two layers of the concentric shields by using six OFHC copper posts. These posts create the magnetic separation and also provide a good thermal path for cooling the JJA chip-mounting surface. Figure 5.2 shows the different layers of magnetic shields used and the complete assembly being used in the JVS system. The magnetic shields are very effective in blocking any kind of

low-frequency magnetic noise from entering the MuMetal® shield enclosure. The low magnetic field enclosure is created by the magnetic shield's physical boundary that separates and isolates the inside volume, but care should be taken in making sure that there is no source of magnetic field present inside the chamber volume. In the operational JVS system, there are potential sources of magnetic field close to the JJA chip. For monitoring the operating conditions of the JJA chip, there are temperature and magnetic field sensors in close proximity of the JJA chip. These sensors are connected to a 19-pin connector mounted on the outer body of the chamber, which establishes connection to the source controller for the sensors. During the operation of the JVS system, the controller was disconnected from the 19-pin connector and a shorting-plug was attached right before the system crosses over the critical temperature of the Josephson junction (9.2 K for niobium junctions).

Figure 5.2: MuMetal® magnetic shield enclosure for the JJA chip.

During the transition from normal conducting phase to the superconducting phase, if the superconducting junctions are exposed to any kind of magnetic flux, it severely affects the electrical performance of the junction. The magnetic flux gets trapped in the

individual junction and hinders the flow of superconducting current. The presence of this trapped magnetic flux reduces the critical current of the Josephson junction. Any significant lowering of critical current is usually a clear indication of flux trapping in the junction. The magnetic flux trapping generally takes place at the transition from normal conducting state to the superconducting state or (for example, when the junction is cooled to a temperature lower than the critical temperature). Hence, it is essential to disconnect and ground all the sensors prior to crossing the critical temperature during cool down cycle. In the case that there is trapped flux observed during the junction operation, the cryocooler must be shut off and the JJA chip allowed to heat up to a temperature higher than the critical temperature until it reaches around 15 K, then cooled down again in the absence of magnetic noise.

The shielding performance of the MuMetal® shields was experimentally observed to achieve levels of 1.4 G or less. Once the MuMetal® shields were designed and fabricated, the system was assembled together and several tests were conducted to analyze the performance. Figure 5.3, shows the results of some of the tests conducted. Magnetic field measurements were done at the location of the JJA chip; these tests were conducted for the following test conditions:

- On Cold Head: Sensor attached directly to the Cold head without any magnetic shielding,
- No MuMetal®: Sensor attached to the chip mount and the chip mount fixed to the cold head with copper-posts providing separation; without any magnetic shielding,
- Outer MuMetal®: Sensor attached to the chip mount and enclosed with one

layer of MuMetal® shielding (outer layer),

- Two MuMetal® shields: Sensor attached to chip mount and enclosed with two layers of MuMetal® shields.

The difference in performance of the different shielding methods is shown in the test results shown in Figure 5.3. The magnetic field present at the JJA chip location is close to 10 G without any shielding at the operating temperature of 4 K and reduces to a value close to 1 G in the case when two layers of cylindrical magnetic shields are used. Further, it can be seen that one layer of magnetic shield also provides a significant reduction in the residue field but is still less effective than both of the layers put together.

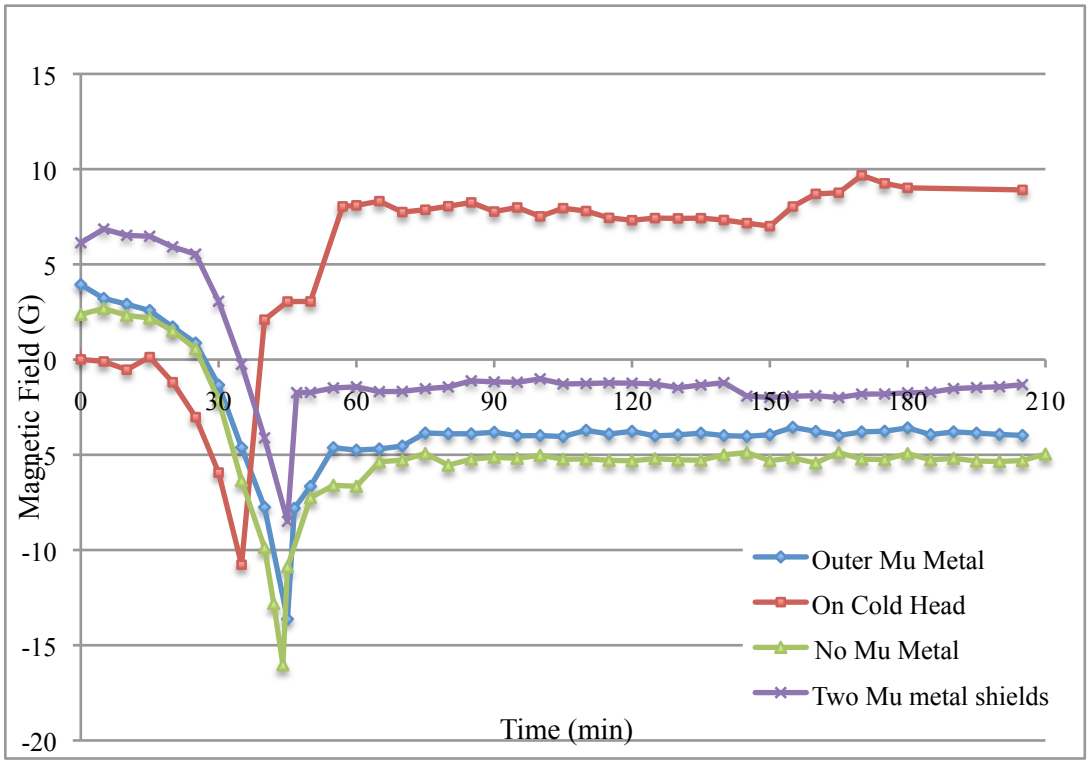


Figure 5.3: Experimental results for different configurations of MuMetal® magnetic shields.

The best indication of the performance of magnetic shielding is provided by stable operation of the JVS system. The value of critical current in the Josephson junction is

highly sensitive to the presence of any external magnetic field and is observed in the I-V characteristic curve of the junction. The specified critical current value of ~110 μA was indicated by the JJA chip manufacturer under the test condition of cooling the JJA chip by immersing into liquid Helium. This critical current value of 110 μA was achieved in the UNC-Charlotte JVS system, and further tests showed highly stable voltage steps which indicated the absence of significant magnetic flux trapping in the Josephson junctions. The results of the operation of the JVS system are discussed at length in Chapter 6.

CHAPTER 6: RESULTS

The assembly of the portable Josephson voltage standard (JVS) system was successfully completed and the system achieved the same performance specifications as that of a laboratory based liquid-helium Josephson voltage standard system. This chapter discusses key parameters associated with the performance characteristics of the JVS system and shows a comparison between the results obtained from the liquid helium-based system and the results from the CCR system for the same JJA chip.

6.1 Performance characteristics for the cryocooler based JVS system

The performance of a JVS system is dependent upon the ability of the JJA chip to attain superconducting temperature. For stable operation of the system it is essential that the JJA chip is kept in an enclosure of very low magnetic field while the wires carrying the measurement signals pass through passive filters to eliminate the influence of radio-frequency interference. The different performance criteria are discussed in further detail.

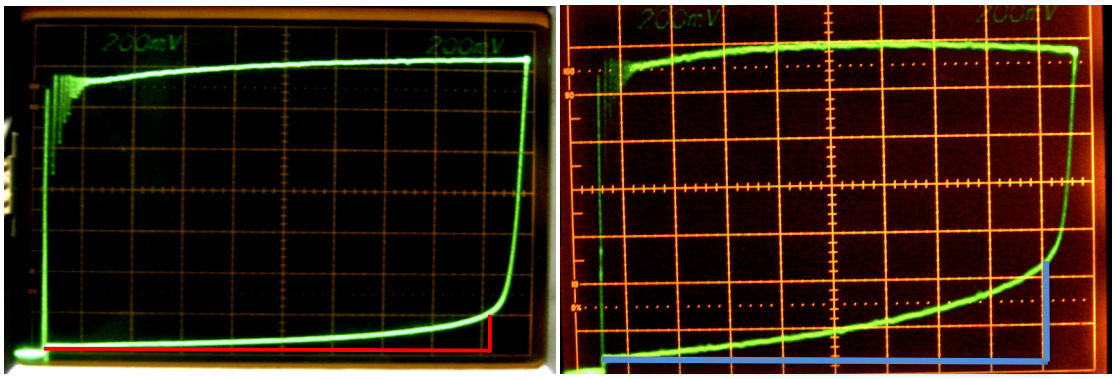
6.1.1 Temperature performance

The operating temperature for the JJA chip is the most critical parameter for the JVS system. The operational temperature attained by the JJA chip can be estimated by observing the leakage current value on the I-V curve. As the temperature of the Josephson junctions starts to rise, the slope of the return loop increases. The advantage of this phenomenon is that it allows the use of I-V curve to assess the actual temperature on

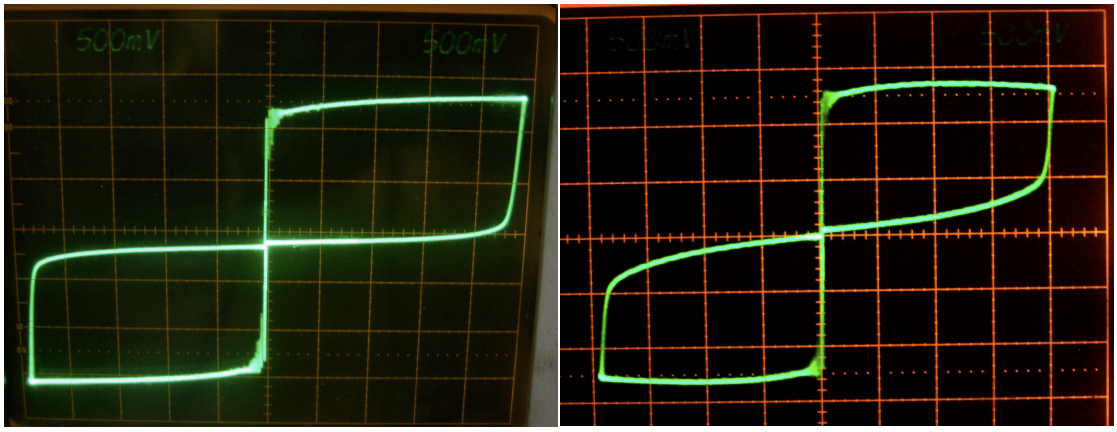
the surface of the chip. Lower slopes indicate cooler chip temperatures, whereas higher slopes indicate that insufficient cooling exists to enable proper operation.

Figure 6.1 illustrates this point. Under normal operation, Figure 6.1 (a), a leakage current of 15 μA is observed at approximately 1.8 V as compared to a leakage current of 40 μA in case of over heated JJA chip, seen in Figure 6.1 (b). As shown in the Figure 6.1 (b), the slope of the return loop is an approximate indication of temperature exceeding 6 K, in this particular case, the chip performed poorly. Figure 6.1 (c) and (d), shows the slope comparison between a JJA chip operating at 4.2 Kelvin and having a temperature higher than 6 Kelvin on a Y-axis resolution of 20 μA/division and X-axis resolution of 200 mV/division. This slope is an indicative temperature, and as the temperature rises, the slope keeps increasing until, at a temperature above the critical temperature of the superconductor, it displays a purely resistive behavior of a normal conductor.

Figure 6.1 (c) shows the I-V curves obtained after cooling the JJA chip on the diamond turned mounting surface and is an indicative of a temperature close to 4.2 Kelvin at the Josephson junctions and shows drastic improvement in the leakage current as compared to the earlier performance on the conventional machined surface shown in Figure 6.1 (d).



(a) Leakage Current of ~15 μA at 1.8 V (b) Leakage Current of ~40 μA at 1.8 V
X-axis → Voltage; 200 mV/div and Y-axis → Current; 20 μA/div



(c) Leakage Current of ~12.5 μA at 2 V (d) Leakage Current of ~50 μA at 2 V
X-axis → Voltage; 500 mV/div and Y-axis → Current; 50 μA/div

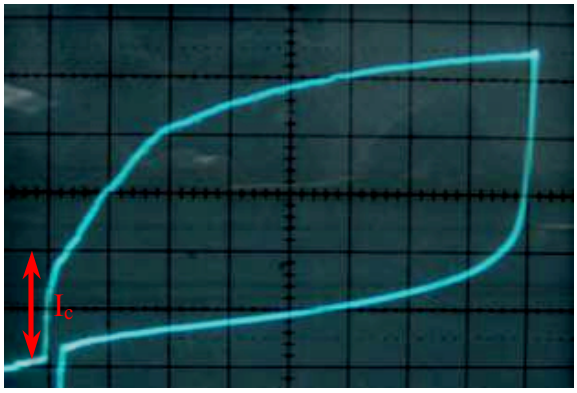
Figure 6.1: I-V characteristic curve as an indicator of operating temperature of JJA chip.

6.1.2 Magnetic Shielding performance

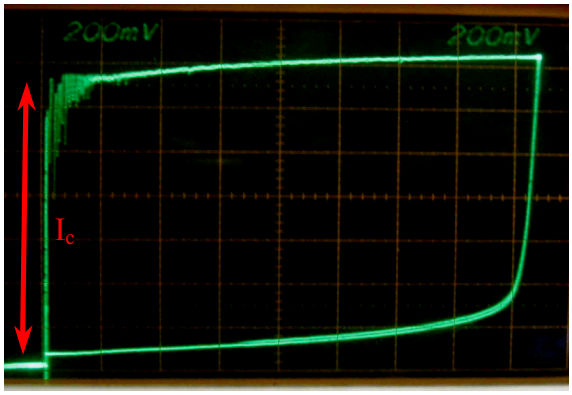
The dependence of magnetic shielding on the performance of the JJA chip was discussed in detail in Chapter 5. The presence of magnetic field at the Josephson junctions causes magnetic flux trapping in the junctions and is directly observed in the I-V curve for the JJA chip. The flux trapping in a Josephson junction reduces the value of critical current for the chip and makes it inoperable. The presence of any magnetic field in the vicinity of the JJA chip is eliminated by the use of MuMetal® magnetic shields. Figure 6.2 (a) shows I-V curve displaying a very low value of critical current, which is a

clear indicator of magnetic flux trapping in the Josephson junction. The trapped flux can be removed by allowing the JJA chip to heat up above the critical temperature and then going through the cool down cycle. Figure 6.2 (b) shows the I-V curve after removal of trapped flux.

The presence of trapped flux in a single junction can completely disrupt the performance of the system. Using a horizontal gain of 5 mV/div., the I-V curve should have a perfectly vertical branch at the origin extending to approximately ±125 μA, as seen in Figure 6.2 (f). Figure 6.2 (e) shows the I-V curve with trapped flux; upon increasing the X-axis sensitivity on the oscilloscope (to 5 mV/div), a breakage in the vertical current line can be seen at a much lower value of ±50 μA than the required critical current.

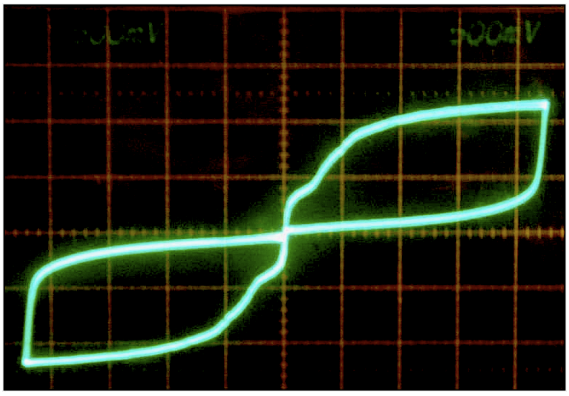


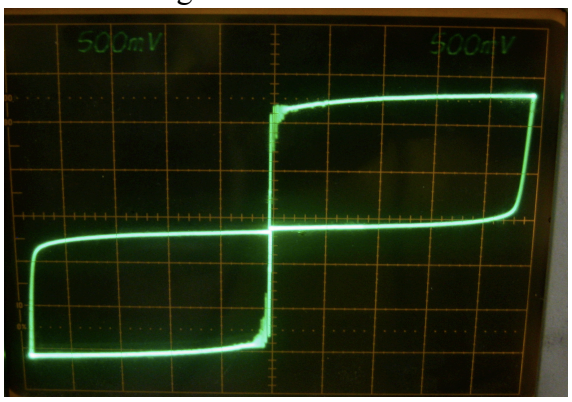
(a): Lowering of Critical Current due to Trapped Magnetic Flux



(b): Critical Current after removal of the Trapped Magnetic Flux

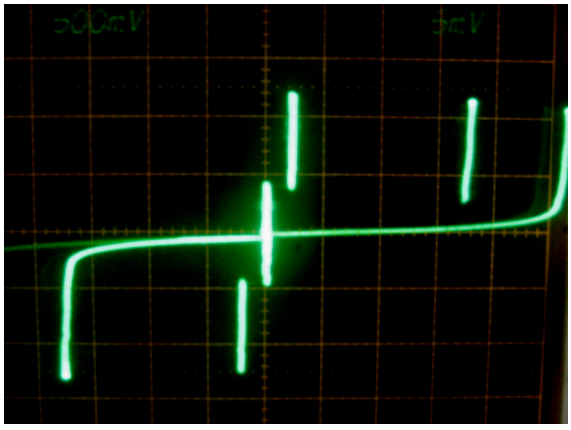
Y-axis: Current → Scale = 20 μA/div and X-axis: Voltage → Scale = 200 mV/div

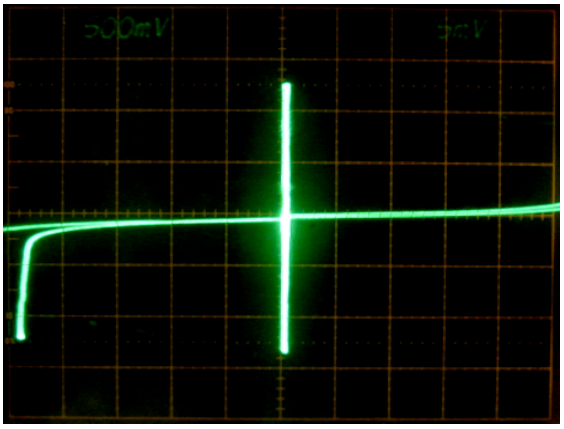




(c): I-V curve with Trapped Magnetic Flux (d): Ideal I-V curve with no flux trapping

Y-axis: Current → Scale = 50 μA/div and X-axis: Voltage → Scale = 500 mV/div





(e): Breaking of current line due to Trapped Magnetic Flux

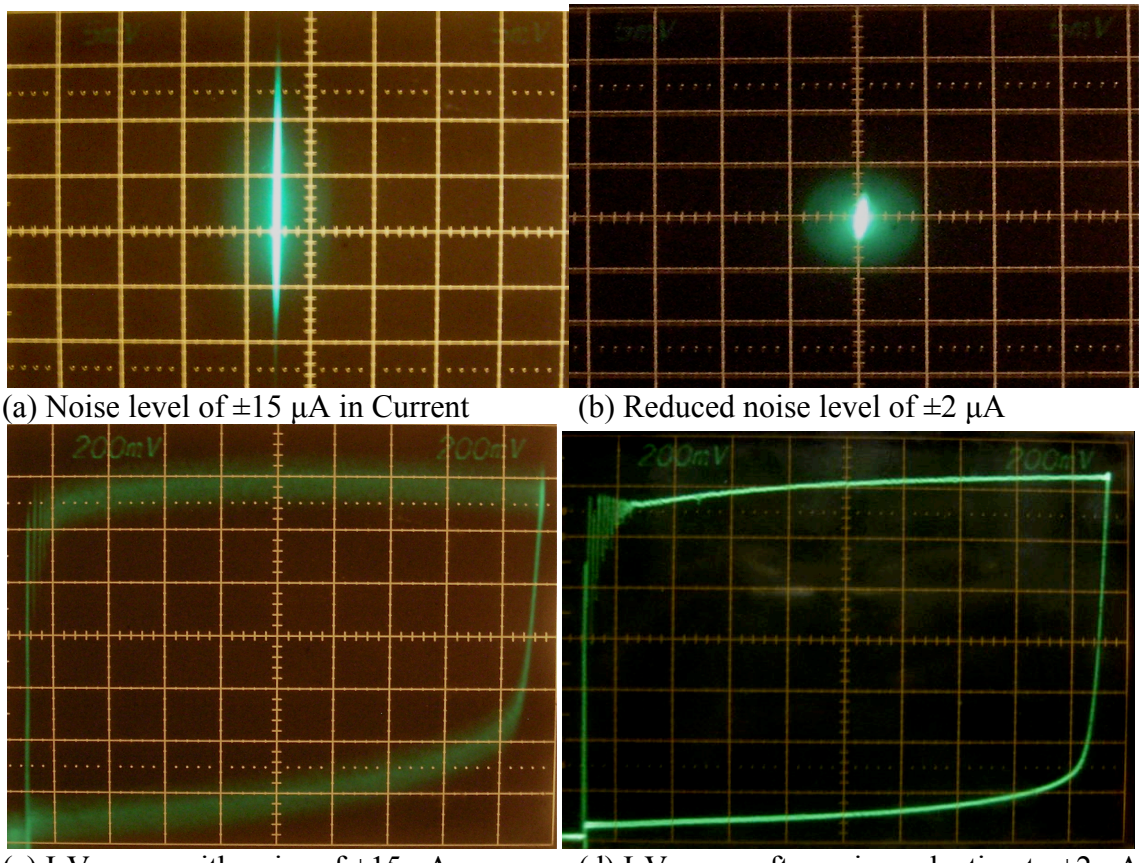
(f): Ideal case, no Trapped Flux

Y-axis: Current → Scale = 50 μA/div and X-axis: Voltage → Scale = 500 mV/div

Figure 6.2: I-V curve of the 1-volt JJA chip displaying magnetic flux trapping

6.1.3 Electromagnetic Noise

The presence of electromagnetic noise can hinder with the stability of the measurement system. If the noise-to-signal ratio is too high, it is difficult for the measurement system to decipher between the two and can cause errors in measurement. Figure 6.3 (a) shows the presence of noise in measurement of current at zero bias. A noise of ±15 μA, seen in Figure 6.3 (a), will affect the I-V curve as seen in Figure 6.3 (c). The electromagnetic noise levels were brought into the acceptable values of ±2 μA, Figure 6.3 (b), by use of passive filters and proper grounding of all the measurement equipment.



(a) Noise level of ±15 μA in Current (b) Reduced noise level of ±2 μA

(c) I-V curve with noise of ±15 μA (d) I-V curve after noise reduction to ±2 μA

Figure 6.3: Electromagnetic Noise levels in the measurement system.

6.2 Josephson Voltage Standard Operational Tests

The accuracy of operation for the portable Josephson voltage standard system based on a 1-volt JJA chip was confirmed by a series of tests performed under various operating conditions. NISTVolt (registered trademark of NIST) is a Windows based software product developed at NIST, in Boulder, CO that is used in acquiring and analyzing data for a Josephson voltage standard system [51-53].

After connecting all the instruments to the system it is necessary to obtain certain system specific information. The following tests are performed after the initial setup of the system and results for the UNC Charlotte-JVS system provide crucial information about the system performance and analyzes the presence of any external noise and interference.

6.2.1 Frequency Uncertainty and Correction

The accuracy of the JVS is dependent upon the accuracy of the frequency reference. Any error in the 10 MHz frequency reference translates directly into an error in measured voltage. It is therefore very important to know the uncertainty and the correction value for the frequency reference. The typically accepted values for a JVS system [51-52] and the values measured for the UNC-Charlotte are displayed in Table 6.1.

Table 6.1: Frequency Uncertainty and Correction values.

	UNC-Charlotte System	Recommended Value [52]
Frequency Uncertainty	0.0001 parts in 10^6	0.00013 parts in 10^6
Frequency Correction	0.000 parts in 10^6	0 parts in 10^6

The above system parameters were measured by utilizing the NISTVolt software and the values obtained for the UNC-Chralotte setup is a match to the required values; hence, the system is well within the operational parameters.

6.2.2 Self Test with 10 kΩ test box

Self-Test is a feature in NISTVolt that allows measurement of 15 different system parameters and displays the measured values along with acceptance values. The system computer communicates with the JVS 1002 controller and provides continuous data during operation. The resistance of the Josephson junction array at room temperature is measured to be 8.9 kΩ; during the self-test a Bias test box is utilized and the testing is done for a 10 kΩ resistor rather the actual JJA chip. The results from the 10 kΩ test box provides an estimate of the noise levels in the measurement system. A comparison between the recommended typical results and the results measured for the UNCC system with the 10 kΩ test load, are shown in Table 6.2.

Table 6.2: Self test measurement results for 10 kΩ test load [51-52]

Measurement	Measured value for the UNCC system	Recommended Range	Compliance
Zero Step, Shorted DUT Null Voltage.	0.22 μV	-1 μV to +1 μV	Good
Array Minimum Critical Current.	1 μA	0 μA to +4 μA	Good
Array Critical Current at 5 V.	495 μA	450 μA to 550 μA	Good
Array return current at 4 V.	397 μA	350 μA to 450 μA	Good

The above measured parameters give an understanding of the measurement capabilities of the instrumentation setup. Any errors or noise in the measurement system would directly translate to the final measured values, because of this reason first the system parameters are checked without connecting the JJA chip to check and measure the offsets and error in these values. As shown in Table 6.2, the measured values of null voltage, minimum critical current, critical current at 5 V and the return current at 4 V are

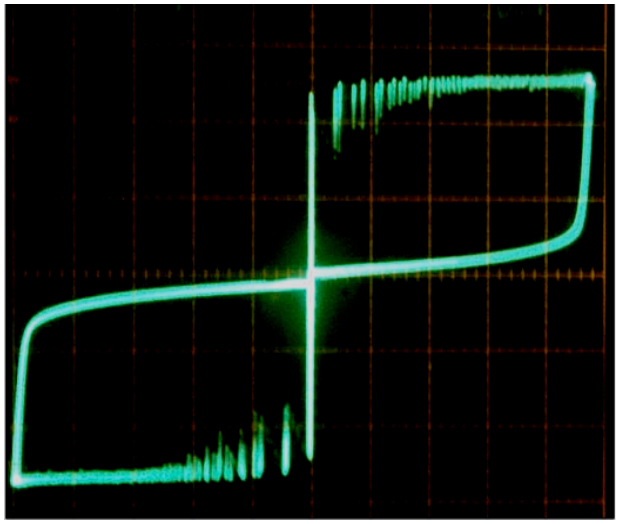
all within the recommended range; this gives an indication that the electrical connection in the system are done correctly without much influence from external noise.

Once the self-test values are all within the accepted tolerance values, the JJA chip is connected to the system and cooled to the appropriate temperature. After the JJA chip has reached the operating temperature of 4.2 Kelvin the values corresponding to the JJA chip are measured.

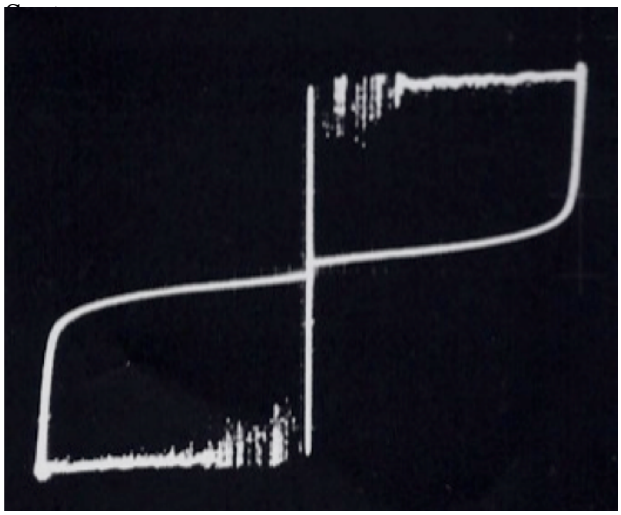
6.2.3 I-V curve for the JJA Chip

The current-voltage (I-V) characteristic curve was obtained after cooling the JJA chip by mounting it on the diamond turned surface of the chip-mount. For proper operation of the Josephson voltage standard system, one of the most important characteristics is the value of critical current of the array. The best way is to compare the performance of the system by visually comparing the I-V curves obtained from the CCR compared to that of the I-V curves obtained from the same chip using the liquid helium Dewar. A good thermal contact between the chip and the chip-mount is illustrated by the critical current value of the I-V curve. The critical current value of the JJA chip measured on the I-V curve is approximately 110 μA; it matches with the critical current value obtained for the same chip (# 2629B11) provided by the manufacturer, Hypres, Inc., which was tested with a liquid helium system.

Figure 6.4 (a) illustrates the I-V curve obtained for the JVS system after diamond turning the chip mount surface; for comparison purposes, Figure 6.1 (b) shows the I-V curve measured in a liquid helium cooling system with the same chip. The critical current value for the UNC-Charlotte system is ~ 120 μA and the leakage current at 200 mV is ~ 15 μA which is comparable to the values obtained from the liquid helium based system as



(a): I-V curve from the CCR based UNCC-JVS



(b): I-V curve from the liquid helium based cooling

Y-axis: Current → Scale = 50 μA/div
X-axis: Voltage → Scale = 50 mV/div

Figure 6.4: I-V curves for the Josephson Voltage Standard System.

110 μA and 25 μA at 200 mV.

Table 6.3 shows a comparison of the important parameter values between the UNC-Charlotte JVS system and the values measured in the liquid helium system. The critical current values is a very important parameter in the JVS system and it provides and indication is magnetic flux trapping in the Josephson junctions. The measured value of 112 μA for the UNCC system shows a marginally better (~2%) performance than the required value of 110 μA obtained in liquid helium system. The critical current value at 5 V also shows a better performance (~ 8%) with a current value of 140 μA as compared to the value of 130 μA for the liquid helium system.

Table 6.3: Comparison of system parameters for the UNCC-JVS system and helium Dewar system.

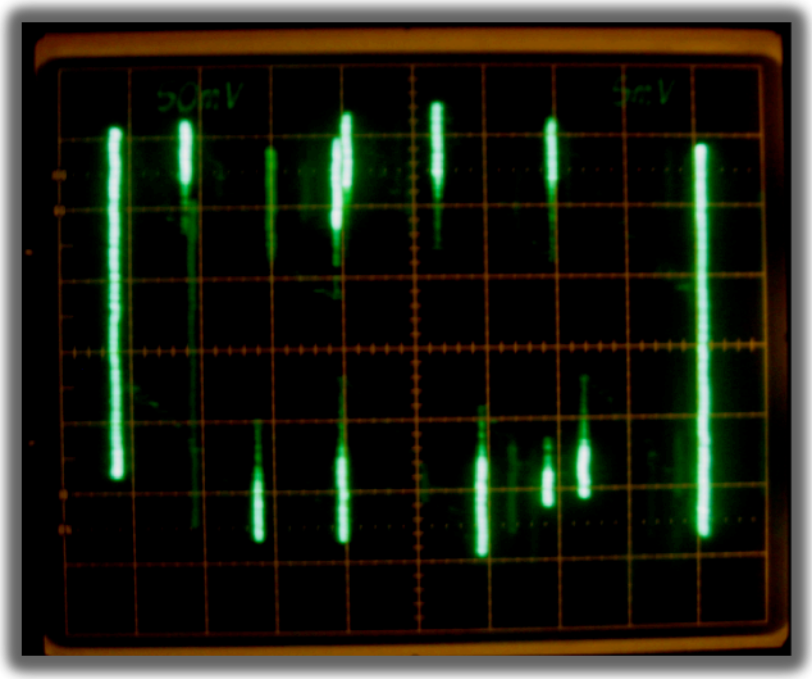
JJA chip # 2629B11	UNCC- JVS	Liquid Helium System	Performance of UNCC system
Minimum Critical Current	112 μA	110 μA	Better
Critical Current at 5V	140 μA	130 μA	Better
Leakage current at 4V	~ 10 μA	~ 6 μA	Acceptable
Room Temperature Array resistance	8.9 kΩ	8.9 kΩ	Same
Frequency of Operation	76.486 GHz	75.66 GHz	N/A
Step Amplitude	~ 27 μA	~ 29 μA	Acceptable
Maximum Stability	105 minutes	449 minutes	Acceptable

The “leakage current at 4 V” is a benchmark of the I-V curve and is the lower intersection of the hysteretic I-V curve with the +4 V grid line. Values greater than 10 μA are indicative of a damaged array or, more usually, a warmer than normal chip. The value

of 10 μA obtained in the UNCC system is indicative of a temperature higher than the liquid helium temperature of 4.2 K. Based on discussions with Dr. Clark Hamilton at NIST/VMetrix and the technical team at Hypres, Inc., it was concluded that, even though the temperature of the JJA chip may be a little higher (approx 4.5 K), the ultimate test is the critical current value and the voltage step stability. As the temperature of the chip rises, the four-volt return current will rise slowly toward 15 μA, at which point the array typically becomes too unstable to use. The maximum stability on a voltage step was measured to be 105 minutes, which seems to be much smaller compared to the step stability obtained in the liquid helium system, but the absolute required value to perform the calibration operation using the JVS system is in the ballpark of 1 minute. Hence, the stability of the system is well within the acceptable operational value. The critical current value, the I-V curves and the voltage step amplitude for the UNCC system were very close to the expected values and hence the operation of the JJA chip was deemed to be very stable.

6.2.4 Voltage Steps

The I-V characteristic of the 1-Volt JJA chip under microwave irradiation is shown in Figure 6.5. The achievement of a proper dc I-V curve is indicative of an efficiently operating cryocooling system with no apparent interference or external noise. Once the I-V curves are obtained, the microwave power is gradually applied to the chip. To adjust



Y-axis: Current → Scale = 5 μA/div
X-axis: Voltage → Scale = 5 mV/div

Figure 6.5: Voltage step representation for a 1V JJA chip with an incident 76.5 GHz microwave power.

the microwave power to the optimum value the sweep amplitude is set to zero and the coarse dc offset to 1 V. The power level is adjusted to maximize the vertical step amplitude. When the complete Josephson voltage standard system is operating with the optimum microwave power applied to the JJA chip, we achieved the results shown in Figure 6.5. This response is an ideal output for the JVS system.

CHAPTER 7: CONCLUSIONS

A self-contained, fully portable, prototype voltage reference standard system has been designed, developed, and tested. The voltage standard system utilizes a Josephson Junction Array (JJA) integrated circuit chip to attain the standard voltage. Unlike typical Josephson junction systems, the system developed in this work was developed for field operation, and utilizes a unique cryocooler configuration in lieu of a helium Dewar to maintain the cryogenic temperatures required for operation. The cryocooler-based system, referred to as a closed cycle refrigerator (CCR) system, enables use of the calibration standard on vehicles such as the US Army's AN/GSM 705 calibration vans.

The introduction of an active cooling system in lieu of the passive helium bath presented many challenges that were overcome through carefully engineered components and new chip mounting techniques. Requirements for a cryocooler-based system are stringent, so a systematic design philosophy was developed to aid in the widespread adoption of such systems. Two dominant areas of concern were identified, precise thermal management and the systematic elimination of electromagnetic noise.

Typical liquid helium Dewar based systems achieve the required cooling (<4.2 K) through three-dimensional convective cooling in the helium bath. In this work, a methodology was developed for mounting the chip on the cryocooler cold-head without the use of adhesives or greases while still ensuring sufficient thermal conduction to maintain the temperatures required for superconduction. Relying only on conductive

cooling of one side of the chip, an innovative chip mount was designed and machined using a state-of-the-art diamond turning technique to reduce the surface roughness of the chip-mount surface and improve the thermal path to the chip.

The use of a CCR based system and the assembly of all the instrumentation electronics in a portable rack brings sources of electromagnetic noise in close proximity of the operating JJA chip. The operation of a JJA chip is very sensitive to the presence of any static magnetic field of even a few Gauss. High permeability MuMetal® magnetic shields were designed and used to create an enclosure that reduced the magnetic fields to less than 2 Gauss. Performance deterioration often occurs due to the presence of electromagnetic noise induced by the cryocooler, motor, pumps, etc. In this work, detailed experiments were conducted to quantify the magnetic fields in the system, understand their effects, and systematically eliminate them. Also, the portable JVS system operating outside the lab environment will constantly be exposed to other sources of noise; to reduce the interference from noise sources magnetic shields and radio-frequency interference filters were incorporated into the system design.

The operational capabilities of the assembled CCR-based JVS system were compared with the liquid helium-based JVS system. Results indicate that the CCR-based system obtained the same values for critical current and voltage step amplitude as the Dewar system. These are the two most critical parameters in assessing the performance of the system. Other parameters, including leakage current value and voltage step stability were found to be degraded in performance, but were still well within the acceptable range. In this case, the CCR-based system had a voltage step stability of 105 minutes, whereas the Dewar-based system had 449 minutes. However, the requirement for stability is less than

1 minute, [73, 74] so the CCR-based system was deemed to be as good as the Dewar-based system for overall performance and provided the portability to be used in outside lab environments and other places where liquid helium is difficult to maintain.

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